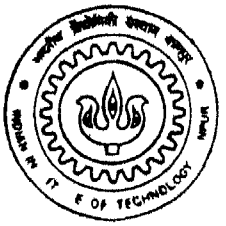
CAPACITANCE BASED CHARACTERIZATION OF PROCESS INDUCED DEFECTS IN N- AND P-SILICON

By

sangeeta swain



MATERIAL SCIENCE PROGRAMME

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CAPACITANCE BASED CHARACTERIZATION OF PROCESS INDUCED DEFECTS IN N- AND P-SILICON

A Thesis Submitted
in Partial Fulfillment of the Requirements
for the degree of

MASTER OF TECHNOLOGY

by

sangeeta swain

MATERIAL SCIENCE PROGRAMME
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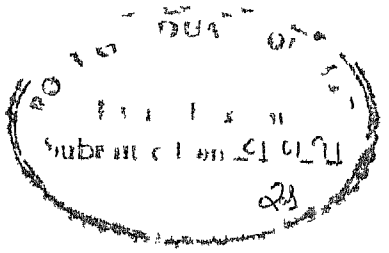
KANPUR JANUARY 1999

DEDICATED

to

My Parents



CERTIFICATE

It is certified that the work contained in the thesis entitled **Capacitance based characterization of process induced defects in n-and p silicon"** by Miss Sangeeta Swain has been under my sypervision and has not been submitted elsewhere for a degree

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Department of physis
Indian Institute Of Technology
Kanpur

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Need not to acknowledge but all the little content that my M techthesis holds within its polythene coverage & all are just impossible without my respected SIR my thesis adviser **Dr Y N Mohapatra** This thesis is nothing but a package of his multifrequency precious advices I have learnt a whole lot of things from him which will definitely come a long way in my life

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SANGEETA SWAIN

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ABSTRACT

Since electron cyclotron resonance (ECR) plasma of hydrogen is emerging as a popular processing technique in silicon technology there is a need to study its effect on the electrical properties of the material Such etching techniques requiring low energy ions normally are used in conjunction with a suitable annealing method such as rapid thermal annealing (RTA) and furnace annealing(FA) In this study we examine the effect such processing steps on electrical manifestation of surface damage hydrogenation and introduction of traps Capacitance based characterization methods such as C V characteristics at different temperature deep level transient spectroscopy(DLTS) thermally stimulated capacitance (TSCAP) technique and time analysed transient spectroscopy (TATS) have been used Metal semiconductor diodes made from material having undergone suitable combination of the processing steps are used for the study Four sets of samples for each type (n & p) are characterised for comparision purposes

For both n and p type silicon ECR hydrogenation alone using a remote plasma does create damage in sufficient amount so as to modify the built in potential severly Though no hydrogenation in the bulk is observed the zero bias depletion layer of schottky diode increases a large amount due to carrier removal and interfaces Following ECR hydrogenation if the samples are subjected to RTA annealing at 500°C for 5 seconds there is almost complete recovery of the C V characteristics This is found to be true for both p and n type samples Following ECR hydrogenation if the furnace annealing at 500 C for 10 min is carried out then there is severe deactivation of dopants for n type silicon even in the bulk The depletion width widens both due to surface damage and carrier removal C V characteristics of Schottky diodes indicate an unusually large built in potential due to modification of the interface In contrast for p type silicon furnace annealing does not lead to such effects and seems to be comparably efficient to RTA Except for ECR etched and furnace annealed samples no other sample of n type set showed any trace of deep levels of less than $1\times10^{12}cm^{3}$ In ECR cleaned and furnace annealed sample of n type a minority carrier trap was observed with both DLTS and TATS DLTS lineshapes were broadered than that of a exponential transient case and yielded an activation energy of (E_V+0 38)ev Similar analysing using TATS did not show any noticeable broadening and the measure emission signature was slightly different yielding an activation energy 0 32ev The broad DLTS lineshape of the minority carrier is attributed to possible temperature dependence of series resistance since the bulk had suffered severe deactivation of dopants The appearance of a minority carriers is due to type conversion in the interface region during furnace annealing Similar phenomena seem to appear in MeV damage created in n Si after 400 C furnace annealing Though with different emission signatures a predominant minority carrier trap also observed along with two majority carriers in that case The minority carrier trap is attributed to complex point defects arising out of migrating intrinsic defects in silicon from the surface damage during furnace annealing No evidence of any deep traps were found in p type samples in the bulk to a concentration of 3×10^{12} cm^{3}

CHAPTER 1

1 1 INTRODUCTION

In the material science of silicon, careful study of effects due to processes involved in technology has played a vital role Most processes have influences both desirable and undesirable On electrical properties of silicon Hence techniques of studying electrically active defects and other electrical manifestation of damage and disorder have been central to this endeavor Ion assisted dry etching processes are currently well entrenched in Si VLSI circuit due to their anisotropy which enables submicron pattern delineation Manufacturers of electronic devices must achieve and maintain proper control of hydrogenation passivation damage creation etc This being the case a great many workers have explored many strategies in hopes of achieving this goal Recently electron cyclotron resonance excited plasma has emerged as a popular choice of cleaning surfaces as an attractive alternative to wet etching and other dry etching techniques In order to minimize damage due to physical impact light ion such as H^+ is the preferred choice for the plasma Since the level of plasma is controlled by the energy of the ions involved ECR H technique provide a better potential alternative to the more conventional techniques involving rf plasma Also one can control both energy and flux independently in an ECR system Hence it is not necessary to increase energy of the ions to obtain better etching efficiency It has recently been shown that ECR excited hydrogen plasma can remove native oxide on silicon in matter of minutes

However presence of hydrogen leads to issues related to hydrogenation which can neutralize shallow donors and deep level defects and generate new defect centers in the material Since ECR plasma creates damage in the presence of hydrogen recently there have been several studies on the simultaneous presence of disorder soaked with hydrogen Some interesting results on hydrogen migration and defect kinetics have been observed In brief it has been observed that the disordered region inhibit hydrogen migration but act as a rich source at later stages of high temperature processing ECR hydrogen plasma cleaned

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silicon develops a set of new traps in the band gap on annealing following ECR etching These results are reviewed in chapter 2 in greater detail

1 2 AIM AND SCOPE OF THIS WORK

In this work our main aim is to isolate the electrical effects of ECR hydrogen plasma etched silicon used in conjuction with thermal annealing processes such as rapid thermal annealing(RTA) and furnace annealing(FA)

The study uses a set of carefully prepared crystalline silicon samples consisting of (i) annealed unhydrogenated controls (ii) ECR hydrogen plasma etched (iii) ECR hydrogen etched followed by RTA and (iv) ECR etched followed by furnace annealing samples one set for each type (i e n and p) have been used

We limit this work to capacitance based methods to characterize metal semiconductor contacts and study of deep levels using techniques based on capacitance transient such as deep level transient spectroscopy (DLTS) and related measurements

As already mentioned earlier this work was planned following reports of interesting defect kinetics on a similar set of samples by our collaborators at Pennsylvania state university[23] It was observed that on annealing ECR H plasma etched silicon samples a set of new traps manifest themselves which were not observed after ECR cleanig alone

1 3 THESIS ORGANIZATION

The next chapter gives principles of techniques used in this work and then goes on to give a review of the background and perspective in which the present work must be viewed Since this work is directly related to some of the specific recent results on similar

set of samples we review them in detail Chapter 3 is devoted to deposition of samples and experimental details Chapter 4 presents our main results and discussion and Chapter 5 lists main conclusions derived from this work

CHAPTER-2

PRINCIPLES OF EXPERIMENTS & REVIEW OF BACKGROUND

2 1 INTRODUCTION

The first half of this chapter is devoted to brief description of concepts and principles involving capacitance based characterization techniques The second half is devoted to issues of hydrogenation and disorder specifically the ones directly related to experiments as similar set of samples by our collaborators

2 2 DEFECTS AS TRAPS / G R CENTERS (in general)

The imperfections such as impurity centers & defects in perturbed crystalline semiconductors introduce additional discrete energy states in the forbidden gap While impurities of neighboring columns next to the periodic system have energy levels close to the band edges of the host system (shallow states) and consequently facilitate the generation of free carriers and hence controls the carrier concentration Impurities of other columns introduce energy levels deep in the energy gap(deeper states)act as carrier recombination centers and hence control carrier lifetime These defects can be electrically as well as optically characterized But electrical characterization of these states has been both convenient and appropriate for most applications Basically the electrical signature of these defects are carried out by the energy level scheme and the electrical probabilities between the defect states and conduction and valence states The electrical characterization of deep levels is normally carried out in terms phenomenological parameters of these levels provided by shokley read hall (SRH) model of trapping and recombination processes The basic information that one seeks from such measurements include thermal activation energy(E_T) carrier capture cross section(σ) & concentration(N_T) of profile etc of traps

A deep impurity in crystalline semiconductor may act either as a trap or recombination center depending on the temperature & the various other doping

conditions Each of these defect centers can either capture/emit electron to conduction band or capture/emit hole to valence band If capture of electron from conduction band is followed by capture of hole from valence band then it is called recombination center and the vice versa for generation center The above process can be mathematically expressed as

$N_T = n_T + p_T$

Where N_T n_T & p_T are the concentrations of the total G R centers occupied those occupied by electrons & holes respectively

Traps are impurity centers which are able to capture electrons & holes and detain them in a restricted volume Basically trapping is a fundamental process for energy storage in almost electrically active solids This energy storage is accomplished by the spatial localization of an excited electrons/holes such that the electron or the hole is prohibited from moving freely through the crystal unless supplied with sufficient thermal or optical energy When the trapped electron or hole is released it is free to move until captured by a recombination center or another trap

2 2 1 TRAP DETECTION TECHNIQUE

This section holds all about the trap parameters & qualitatively the experimental techniques that leads us to identify trap centers by following their finger prints hence they left behind However the electrical impressions of the traps can be best obtained by implementing capacitance based techniques in depletion regions of the specimen under test

2 2 1 1 DEFECT CHARACTERIZATION BY C-V TECHNIQUE

The experimental study of deep levels in semiconductors was revolutionized following introduction of capacitance based methods The use of c v measurements is one of the most popular methods of profiling shallow dopants The key to this lies in the dependence of SCR region width on the applied reverse bias Let us recollect the physics lying behind profiling semiconductors for the majority carrier distribution by c v technique

Let us concentrate on the SCR region of the schottky diode having depletion width W applied with reverse bias V(d c) applied to metal side of the junction The capacitance (dQ/dV) is determined by superimposing a small amplitude ac voltage v on the on the dc voltage V[37] The ac voltage typically varies at a frequency of MHz with an amplitude of 10 to 20mv The capacitance of schottky diode is

$$C = A (q \in / 2)^{(1/2)} (N_{SCR} / (V_{bi} \quad V))^{(1/2)} \qquad (2\ 1)$$

Where N_{SCR} is the ionized impurity concentration in the space charge region
It is also assumed that potential drop due to leakage current is small and hence all the reverse biasing potential drops across the depletion region Also assumption are made that diffusion capacitance is negligible compared to the depletion capacitance & no transverse nonuniformities exit

2 2 1 2 CAPACITANCE VOLTAGE PROFILING

A special care is needed inorder to interpret the junction capacitance measurements of a damaged semiconductor having deep centers In a deeply damaged one the trap levels are located above or below the fermi level in p type & n type materials respectively Particularly deep traps have been found to influence apparent free carrier profiles determined by c v measurements

Under the assumption of one sided step junction as in fig(2 1a & 2 1b) shows the resulting band bending of the junction at a given reverse V for the case of deep donors and deep acceptors respectively The unique feature of a structure with deep traps in the region(x y) in which generation recombination processes are active in determining the equilibrium occupation of traps The more general case is exemplified by the rest of the depletion region O_iW_iy which is fully depleted of mobile carriers and in which trap occupation is controlled only through emission processes The existence of these two regions results in a space charge uniformity This nonuniformity is represented by a

staircase function This transition region has a Debye tail of majority carrier which spills into the depletion region This carrier concentration acts to give a finite equilibrium population probability of deep traps in that portion of the depleted region In addition this fuzzies of the depletion width boundary serves to limit the spatial resolution of c v profiles about a Debye length even in materials without deep traps To find majority carrier profile for uniformly doped substrate the equation (2 1) can be written in the form

$$N_{SCR}(x) = 2 / [q K_S \in A^2 \{ d(1/C^2)/d(V) \}] \qquad (2\ 2)$$

with $x = K_S \in A / C$ The trap profile can be extracted from the knowledge of background profile

2 2 1 3 CAPACITANCE TRANSIENT

A huge amount of information have been collected over last two decades about deep levels through transient based capacitance techniques The whole technique is based upon the dependence of junction capacitance of a Schottky device on the space charge region width and hence related to the trap concentration Capacitance transient is basically the excitement of the perturbed system to nonequilibrium state & then monitoring the equilibrium states while allowing the system to relax Under reverse bias the traps in the part of the depletion region are unoccupied A nonequilibrium situation is created by inducing the semiconductor either with zero bias or with forward bias for a short duration The trap levels goes below fermilevel and hence unoccupied traps get filled up On reapplication of the reverse bias the carriers getting emitted from the trap are swept out of the depletion region So the variation of the trap concentration with depletion width is monitored The transient would be exponential one if the change in capacitance is small as compared to the steady state capacitance which can be expressed as

$$C(t) = C_0 [\ 1 \quad (n_T / 2N_d) \exp (t / \tau\ )] \qquad (2\ 3)$$

where C_O is the steady state capacitance at reverse bias n_T is the occupied trap concentration and N_d is the shallow doping concentration τ is the characteristics emission constant of the trap And the emission time constant has an arrhenius dependence on temperature as

$$1 / \tau = \sigma < v_{th} > N_C \exp (E_T / KT) \qquad (2\ 4)$$

Where E_T is the activation energy of the trap σ is the capture cross section of the trap Hence monitoring capacitance at different temperature allows us to determine σ as a function of temperature and hence trap parameters E_T & σ_n Experimental characterization is performed by using Arrhenius plot to obtain the activation energy For $N_T \cong N_d$ or if several traps decay with same emission rate then a nonexponential transient signal do exist

2 2 1 4 THERMALLY STIMULATED CAPACITANCE (TSCAP)

In the reverse biased TSCAP the specimen under test is maintained under reverse bias is induced with zero bias pulse of short duration or forward bias pulse (in case of FORWARD BIASED TSCAP) Hence the system is allowed to attain nonequilibrium state Then it is allowed go through a heating cycle keeping the heating rate almost constant The corresponding steady state capacitance is monitored in the heating cycle as a function of temperature During heating the traps emit carriers and the corresponding capacitance steps are observed in the tscap spectroscopy The mid point temperature of the capacitance steps Tm is related to the activation energy E ($= E_C - E_T$) or ($E_T - E_V$) by

$$E = K T_m \ln [\nu K T_m^2 / \beta (E + 2 K T_m)] \qquad (2\ 5)$$

Where β is the heating rate and ν is attempt to escape frequency The trap concentration can be obtained from step height And activation energy from arrhenius plot with different β

This analysis gives a approximate analysis of energy level & trap concentration compared to other techniques

2 2 1 5 DEEP LEVEL TRANSIENT SPECTROSCOPY (DLTS)

D V LANG[ ] was the first to introduce the rate window concept in the form of dlts to deep level characterization Capacitance transient have been widely utilized for deep level relaxation studies DLTS converts the exponential transient into a spectroscopy If the c t curve from a transient capacitance experiment is proceeded so that a selected decay rate produces a maximum output then a signal whose decay time changes monotonically with time reaches a peak when the rate passes through the rate window with of a boxcar averager or the frequency of lock in amplifier When observing a repetitive c t transient through such rate window while varying the decay time constant by varying the sample temperature a peak appear in the temperature vs output plot is named as a DLTS spectrum This peak is shown as in fig (2 2)

Let us understand the dlts using capacitance transient The c t wave form of a capacitance transient follows the exponential transient as in equation (2 2) as

$$C = C_0 [\ 1 \quad n_T(o)/(2N_D \exp(\ t/\tau\ )\ ] \qquad (2\ \ 6)$$

with te dependence on temperature as

$$\tau = \exp [\ (E_C \quad E_T) / KT] / (\nu\ \sigma\ T^2\ ) \qquad (2\ \ 7)$$

In BOXCAR DLTS technique c t waveform are sampled or gated at times $t=t_1$ and $t=t_2$ and that the capacitance difference $C(t_2)$& $C(t_1)$ is the standard output feature of a double boxcar instrument There is no difference between the capacitance at the two sampling times for very low or very fast transients corresponding to low & high temperatures A difference signal is generated when the time constant is of the order of the gate separation (t_1 t_2) and the capacitance difference passes through a maximum as a function of temperature This is the DLTS peak The capacitance difference or DLTS signal is obtained by weighing function $W(t) = \delta(t \quad t_1)-\delta(t\ t_2)$ in

$\delta C = (1/T) \int_o f(t)\ W(t)\ dt$

where f(t) is the capacitance signal at temperature T_1 $\tau_{e,max}$ given by $\tau_e$max = (t_2 t_1)/(ln(t_2/t_1)) this is independent of magnitude of capacitance and the baseline of the signal need not to be known Setting of t_1 and t_2 can be done by (i) t_1 fixed vary t_2 (ii) t_2 fixed vary t_1 (iii) t_2/t_1 fixed vary t_2 t_1

Last is preferred to earlier because magnitude remain same in size and shape It has been experimentally found that the sampling or gate width should be relatively wide because signal/noise ratio is proportional to the square root of the gate width Impurity concentration cannot be determined from dlts signal because this does not give capacitance step Trap concentration is given by

$$N_T = (\delta C_{MAX}/Co) 2N_d (r^{(/ 1)} / (1 r) \qquad (2 8)$$

where r = t_2/t_1 If dlts is carried out with the specimen is given a forward bias i e metal semiconductor junction of the schottky device is forward biased then this is called FORWARD BIASDLTS

2 2 1 6 TIME ANALYZED TRANSIENT SPECTROSCOPY (TATS)

This is an isothermal technique where time window is varied keeping the temperature constant unlike dlts where temperature is varied keeping the time window fixed TATS is one such isothermal spectroscopic technique based on difference signal in time window The TATS signal is given by

$$S(t) = C(t T) \quad C(t+\gamma t T) \qquad (2 9)$$

where C represents the isothermal capacitance transient at temperature T and γ is an experimentally chosen constant For exponential transient of time constant τe S(t) has a max when plotted against ln(t) and max time tm is given by the relation

$$\tau = \gamma t_m / \ln(1+\gamma)$$

The peak value of TATS is given by

$$Smax = Co (N_T/2N_{d)} (\gamma / 1+\gamma) (1 + \gamma)^{1/\gamma} \qquad (2 9)$$

where Co is the prefactor of the transient C(t T) There are several advantages of TATS analysis over DLTS TATS is a spectroscopy in the time domain alone so there is a least possible of the transient prefactor dependence upon the temperature In DLTS the line shape is dependent on trap parameters where as the trap peak depends only upon the parameter γ which is chosen to optimize resolvability and signal to noise ratio

2 3 TECHNIQUE OF DAMAGE CREATION

Ion implantation has proved to be extremely useful in advance materials processing and integrated circuit fabrication However the process lead to generation of defects which unless removed degrade the device performance The nature of defects created depends upon the mechanism of interaction and the energy of the collision of the ions

2 3 1 PLASMA SOURCE ION IMPLANTATION

The technological importance of ion implantation is well established due to its diverse applications in improving the mechanical electrical and optical properties of the materials In the ion implantation process the ions are accelerated to high energy (10Kev --few hundreds of Kev) and are injected in the solids This process not being controlled by thermodynamic constraints can also be used to produce new localized phases depending upon the application

Plasma source ion implantation(PSII) is relatively a new technique and represents a radical departure from the conventional ion implantation technology The PSII technique circumvents the inherent line of sight restriction as in case of conventional ion implantation In PSII targets to be implanted are kept directly in a plasma source and then biased to a high negative potential A plasma sheath is formed around the target and the ions bombard the entire target PSII has been used for a variety ofg semiconductors and metallurgical applications

Normally hydrogen annealed by either high voltage DC or more frequently by rf alternating voltage This a rapid thermal anneal(RTA) process in which the implanted layers can be annealed out using laser beams of energies nearly 1-100 J/cm 2 The sample

to be annealed is placed inside a cylindrical tube with He lasers sitting arround it The annealing is carried out by putting the He lasers ON suddenly for few min Because of short duration of heat the profiles of the implanted impurities may be annealed without appreciable diffusion The verginity of the sample can be acquired fully is the advantage of RTA over furnace annealing However furnace annealing(FA) is the convenient method of annealing Now a days RTA techniques include pulsed lasers(pico sec) pulsed electron and ion beams scanned electron beams high beam current implants and broad band spectral sources (high intensity lamps) with fast programmable anneals

2 4 LITERATURE SURVEY

2 4 1 A BRIEF REVIEW

We now review issues related to hydrogenation and hydrogenation in the presence of disorder created by various specifically ECR excited hydrogen plasma

2 4 1 1 HYDROGEN RELATED & HYDROGEN INDUCED DEFECTS

A survey of the phenomena associated with a hydrogenated Si semiconductor is presented in the following in brief trying to provide a simple and coherent general formulation of the problem and review the current state of the subject and a suggestion for further progress The fundamental understanding of hydrogen related defects in semiconductors has proved greatly in recent years due to the strong interaction between experiment and computational theory

Hydrogen has gained recognition as an important impurity in semiconductor and can be introduced intentionally or unintentionally during crystal growth or many of the subsequent stages of the device processing Hydrogen being ubiquitous in the environment and since atomic hydrogen diffuses rapidly and highly reactive makes the electronic devices manufacturers more curious about it and has gained its own position in this world

H is extremely effective in passivating semiconductors As it is light and small it rapidly diffuses through most solids Of course it may take more than one hydrogen atom to passivate vacancy complexes and H_2 molecules may be present in the larger ones And once the defect get passivated by hydrogen annealing at higher temperature required to reactivate that damage

JOHNSON et al [1] reported that atomic hydrogen neutralizes deep impurities and shallow donors/acceptors Also form complexes with donors/acceptors & induced defects in Si

Hydrogen passivation of deep level defects has been demonstrated with DLTS for the n Si oxygen related thermal donor (TD) (where the defects were generated by furnace annealing of 450 C for 1hr) defects in Si [2] Passivation is manifest by the decrease in the DLTS signal after hydrogenation of the sample which after correction for changes in the spatial interval within which deep levels are detected corresponds to a decrease in the near surface density of TD centers They interpreted this as passivation involves H bonding at the TD site so as to alter the electronic states of the defects as manifested by a shift of the energy level When the level is removed from the semiconductor band gap this effect is commonly reffered as hydrogen neutralization of an impurity or defect

Sab et al [3] and Pankove et al [4] [5] discovered that shallow acceptors in Si could be passivated by atomic hydrogen In the experiment by Sha et al [3] the source of hydrogen was an oxide layer on the Si surface whereas Pankove et al [4] [5] sample was exposed to a hydrogen containing plasma Both groups found that a high resistivity surface layer was formed by the diffusion of hydrogen They compared the spreading resistance profile before and after hydrogenation and concentration of boron and deuterium measured by SIMS It was found that the depth of high resistivity surface layer corresponds to the depth of deuterium incorporation measured by SIMS i e the increase in resistivity induced by hydrogenation is accompanied by migration of the hydrogen into the material

Several theoritical calculation [6] in P Si the lowest energy site for isolated hydrogen is at the bond center between two Si atoms From the plot of formation energy for different charge states vs fermi level position hydrogen has a donor state in the upper

half of the band gap The hydrogen passivation of an acceptor impurity has been envisioned as first involving the compensation of the shallow acceptor by an hydrogen donor[7] The charged H^+ is then atttacted to the ve acceptor this long range coulomb attraction drives pairing of acceptors with mobile H^+ The final product is a acceptor-H complex in which covalent bond plays a dominant role

Pankove et al [8] suggested bond center(BC)structure for B H complex in Si They observed a vibrational absorption band at 1875 cm^{-1} for the complex They argued that 1875 cm^{-1} frequency was more typical of a Si H bond than a B H bond Hence they proposed that H was attached primarily to a Si atom and that the H atom interrupt Si B bond to leave the B atom tricoordinated Also DeLeo & Fowler [9] found the total energy of B H complex was minimized for at BC site by cluster methods

Johnson et al [11] observed the passivation of shallow donors by hydrogen by doing hall measurements on n si They observed a decrease in the free electron density after hydrogenation was accompanied by the increase in effective hall mobility which is consistent with reduced ionized impurity scattering due to neutralization of the donor dopants Thus shallow donors get passivated by hydrogenation

The infrared absorption measurement by Bergman et al [10] confirms the existence of donor H complex and that in the case of H passivated donor the independence of the vibrational frequencies upon the identity of the donor confirms the symmetry of donor-H complex Total energy calculations [12] agree in that the lowest energy configuration is realized when H is attached to Si atom at the AB(anti bonding) site

The dissociation of Acceptor H complexes in junction field of a Schottky barrier diode was first studied by Zundel et al [13] From the conc profile of active acceptors through C V measurements they found that annealing in the presence of reverse bias act to sweep H^- from near surface region of the junction This was interpreted as with annealing the acceptor H pair dissociates which acts to push the passivation region into the junction The dissociation was found to follow first order kinetics The B H dissociation energy was reported as 1 28 eve[13] Bagmen et al [14] reported an activation energy of 1 32 eve for the dissociation of PH complex in Si observing distribution profile of donors

S J Pearton et al [15]observed deep level electron and hole trapping states at (E_C 0 53)ev and (E_V+0 45)ev from DLTS spectrum on n and p type si respectively after plasma hydrogenation at 250 C 300°C This was interpreted that of due to the high concentration of hydrogen incorporation in the near surface region creates sufficient local strain in the lattice which facilitates defect generation He suggested that the effect of a possible vacancy or interstitials created in the near surface region and diffusing rapidly into the bulk might be responsible for the above

The hydrogen can migrate in silicon as a negatively charged species(H^-) J Zhu et al [16] reported the combined observation of a strong electric field dependence in the rate af removal of PH complexes during bias temperature stress of hydrogenated Schottky barrier diodes and resulting spatial redistribution of neutralized donors The detection of H^- establishes that there exists an acceptor level for hydrogen in the silicon band gap

The question of the charge state of hydrogen in n and p type si has been addessed in a number of studies A J Tavendale et al [17] demonstrated the drift of a donor passivating hydrogen species under the action of the electric field in the depletion region of a reverse biased hydrogenated n Si Schottky diode The redistribution is explained by the unidirectional drift of the negatively charged passivating species and is confirmed by SIMS profiling in deuterated diodes The results are consistent with the presence of an acceptor level for hydrogen in n type Si

It has been established that hydrogen migrates interstitially with both positively and negatively charged species Upon trapping by impurities neutral H dopant complexes are formed But self trapping of H is expected to to take place for higher concentration values with the creation of the highly stable H^2 molecules being a natural consequence Indeed while various bonding configurations have been considered most theoritical calculations conclude that the creation of the H H bond lowers the energy of two H atoms and predicts the interstitial site as the preferential location of the H^2 molecule [29 30 31] However the actual existence of H^2 molecules in crystalline Si has never been confirmed by a direct experimental observation[32]

Johnson & Herring[33] reported the presence of an immobile form of monoatomic hydrogen at the p n junction interface on the basis of the SIMS measurements In n+ p

junctions a prominent peak in the distribution appears at the edge of the bias dependent depletion layer in the p type material and in reverse biased diodes a sharp peak also appears in the depletion layer Both the features represent accumulation of hydrogen in excess of the local B concentration Most of the accumulation they found in the form of highly immobile neutral entities They proposed that these are hydrogen pairs H^2

In contrast to this H^2 has been observed in amorphous Si[34] P Stallinga et al[35] reported the EPR spectrum on annealed Si samples implanted with hydrogen and deuterium They identified it as arising from a hydrogen molecule oriented in the <111> crystallographic direction and located probably in the interstitial sites i e which is the paramagnetic state of H^2 molecule This result however is consistent with recent theoretical calculations predicting such an orientation to be of low energy Further the EPR derived evidence that H^2 also experiences interactions with more distant hydrogen atoms indicating the existence of larger complexes

2 4 1 2 ION IMPLANTED HYDROGENATED P-SI (A REVIEW)

With ion implantation defect sites are generated and these defect sites are effective centers for trapping hydrogen Pankove et al [22] have speculated on similar trapping of hydrogen in defects formed by implantation process

The combined effect of hydrogen and disorder (due to implantation)on p-Si was presented by Srikanth and Ashok [18] They used p Si ECR hydrogenated sample The sample was implanted with 20 Kev (1×10^{15}) Ar and 380 KeV (2×10^{15}) to create surface damage region & subsurface damage regions respectively From spreading resistance & SIMS measurements Ashok et al [19] observed that profile is consistent with the spreading resistance & its magnitude in the bulk is progressively reduced with Ar implantation dose This was interpreted as ability of Ar ion implant damage to supress penetration of deuterium into the Si bulk, i e the hydrogen which otherwise would have diffused several μm into Si gets enmeshed wherever the disordered regions are

Ashok & srikanth [18] perfomed experiment on disordered & hydrogenated p Si (RTA anneal)with different substrate resistivity They observed a greatly enhanced

deactivation profile was observed after RTA annealing Thus they interpretted the H⁺disorder layer as an abundant source of H for short annealing time (< 1ms)

They carried out experiment on hydrogenated sample by depositing a thin layer of polycrystalline or amorphous Si The control sample showed acceptor deactivation to a depth 3 μm while complete absence of acceptor deactivation is seen with Poly c Si and 100 nm of a Si Thus a very thin disordered layer is adequate to act as a sink for D & prevent its penetration into the crystalline Si below

They studied the effect of subsurface disordering(380 KeV Ar implant create damaged region close to the implant region) by high energy Ar implant on the hydrogenation process They observed the supression of the deactivation beyond the damage region However near surface upto 0 3 μm shows extensive deactivation since most of the damage concentrated close to the implantation depth They argued that the Ar implant region act as a barrier for H flow hence H get accumulated at the near surface It was observed that after annealing the resistivity and hence dopant deactivation increases on both sides of the implanted region They argued that since there is no extra source of hydrogen during the RTA the enhanced deactivation has occured due to the diffusion of H from the damaged region From this they concluded that the H harbored by the damage is released continuously during anneal and causes deactivation of the nearby regions

The decreasing trend in acceptor deactivation/penetration may be attributed to (i) Fermi level position near the surface (ii) defect site entrapment of hydrogen in the disordered network And the fermi level position alteration by the Ar implant damage could hamper the permeation of hydrogen into the bulk[20]

2 4 1 3 THERMAL ANNEAL ACTIVATION ECR PLASMA CLEANED SI (A BRIEF REVIEW)

At present the processes of rf plasma etching of semiconductors are widely investigated in connection with the great prospects of their application in VLSI technology Interest has also been developed in the study of crystal surface damage by the plasma influence

ECR hydrogen plasma has been found effective in cleaning Si surface in few min with no substrate heating[23]

Plasma exposure could also modify the electrical properties of the substrate thus degrading the properties of the subsequently fabricated epitaxial layers or devices However plasma processes might introduce undesirable effects including metal contamination from sputtering from wall chambers and electrodes physical impact damage and penetration of implanted damage into substrate [24]

Nam & Ashok[23] studied the defects appearing due to ECR H plasma exposure and subsequent thermal anneal The wafers used are 6 in B doped <100> p type czochralski (CZ) si and phosphorous doped <100> n type CZ Si having Schottky structures plasma cleaned/annealed samples

Reverse bias dlts scan on p Si ECR hydrogenated samples of varying duration were observed They observed that dlts peak height increases monotonically with the plasma exposure time The control sample did not show any peak The activation energy was found to be 0 47eV The n Si samples showed a similar single peak with major carrier activation energy 0 42eV They pointed out that all these peaks might be due to incorporation of lage concentration of H and were of extended type In dlts spectra of 4 min plasma cleaned thermal anneal ~ 450 C several well defined peaks with considerably higher concentrations occured for both n & p type Si In n Si four major peaks were with activation energy observed at 0 25 0 36 0 53 & 0 64 ev with respect to the conduction band Thev concluded that thermal anneal helps in dissociating the H donor complexes and hence new defects came out which were previously dormant perhaps due to passivating H species Similarly p Si of 4 min H plasma exposed & 20 min annealed at 500 C showed three major peaks with activation energies of 0 19 0 42 & 0 56 ev Control samples were annealed but no dlts peak was found This confirmed that the impurity contamination during thermal annealing was not responsible for the observed defects Total reflection X ray fluorescence measurements have confirmed that no impurities were added during plasma exposure[26]

Reverse biased n Si samples were tested with different filling pulse heights [23] The control sample did not show any peak at various bias conditions whereas the defect concentrations decrease with filling pulse height i e as one moves towards the bulk They found defects were found to be confined to very narrow region before and after annealing

H plasma can create hydrogen stabilised platelets within 0 1 μm of the surface [25] Also void like defects decorated by hydrogen are formed after ECR plasma exposure at depth uo to 14 nm from the surface of concentrations (~ 10^{20} cm^{3}) This suggest the formation of displacement damage to the Si lattice in the near surface rtegion despite the low mass of hydrogen Johnson et al reported two traps with activation energies of 0 06 and 0 51ev in n Si (without annealing)

Isothermal annealing was performed on a set of samples yield for 500 C of 8min plasma exposed n type sample there is a latent period beyond which the defect concentrations rises abruptly upto anneal time 4hr with a decline after 6hr anneal reveals the thermal stability of the defects

Photoluminescence (PL) spectra of hydrogenated p Si with & without annealing were studied[23] Control sample showed a high grade defect free chracteristics whereas most dominant one was at 1 092ev is the transverse optical phonon replica of the boron bound exiton[27] The peak at 1 028ev is assigned to two transverse optical phonon replica of the boron bound exciton The peak at 1 032ev may due to transeverse acoustical phonon replica of boron bound and 1 082ev peak due to trasverse optical phonon replica of shallow level related transition Annealing of control sample does not change the PL spectrum This again confirms the absence of contamination problem associated with the thermal anneal step A new paek was observed at 0 97ev after plasma exposure for 8min was assigned to a hydrogen related defect[25 28] This get disappears at 500 C annealing Again a broad shoulder appears at 0 74ev and 0 89ev after hydrogen exposure In the earlier study of reactive ion etching of Si with D plasma a broad PL peak at 0 90ev has been reported[29] Further the intensity of peak decreased significantly at peak position of 0 96ev after annealing at 800 C These results were attributed to electron hole pair recombination in a heavily damaged near surface region after plasma exposure The hydrogenated annealed samples chemically etched to remove 1μm of the surface region yield Pl spectra coinciding with the control This confirmed the defects induced were confined to the near surface region only The dlts scan of the CZ (czochralski) and MCZ(magnetic grown CZ) with 10 12 ppma of grown in oxygen and 5 ppma oxygen

concentration showed similar defect spectra thus refuting any dependence on the grown in oxygen concentration in the starting material

The results are also of interest in Si technology where hydrogenating gases are frequently used in plasma etching systems

The experiments in this work have been planned on the basis of above mentioned results using similar samples

CHAPTER 3

3 1 SAMPLE DESCRIPTION & EXPERIMENTAL TECHNIQUE

This chapter is devoted to description of samples and techniques used in this work In the present work our main aim is to study capacitance and current based steady state or transient measurements in the temperature range of 77 330K of hydrogenated and/or annealed samples During the study we have carried the following measurements

(i) capacitance voltage transient(C V) characteristics measurement

(ii) Deep level transient spectroscopy(DLTS)measurement

(iii) Thermally stimulated capacitance (TSCAP)measurement

(iv) Time analysed transient spectroscopy(TATS)measurement

3 1 1 SAMPLE PREPARATION

The wafers used in this experiment are 6 in p type czochralski (B doped) Si and n type czochralski(P doped) Si samples The wafer resistivities are 1 10 Ω cm for P typeand 7 20 Ω cm for n type The schottky contacts of 1 mm^2 area were fabricated on the front sides of the H plasma exposed as well as unexposed control wafers with and without thermal annealing ,Metal masks each having circular holes of 1mm^2 area are used during metal deposition for defining schottkty diode area Au is thermally evapourated through a shadow mask onto the front surface of n type samples & Ti followed by Al for P type samples for schottky contacts Sample preparation is as follows

The ECR system consists up of two electromagnets a 2 45 GHz tunable waveguide a mechanical pump and a turbomolecular pump The power supply to ECR ion source (from ASTBC)was given by a microwave power of 600W The sample was kept away from the ion source The base pressure was 10^{-6} Torr and at the hydrogen gas flow rate of 2 8 sccm the operating pr was 0 15 mTorr

The basic priciple involved in ECR is ions are allowed to revole in magnetic field so that they attain a resonance state and hence the corresponding cyclotron

Hence these hydrogen gas get ionized The sample was kept in this plasma atmosphere and hence get plasma cleaned The sample preparation upto this step was done at pennsylvania state university of electronic materials and processing research laboratory

3 2 EXPERIMENTAL SETUP

As far as the main work is concerned we have to study and measure the capacitance as a function of temperature time and voltage Except for the temp programming the whole set up is computer controlled and is common for transient as well as steady state measurements

3 2 1 SAMPLE MOUNTING

The wafers are cut into convenient sizes and mounted on the standard TO5 header for measurements The contact from metal area of schottky diode is taken with a very fine gold wire (25μm dia) bonded with polymer based conductive silver paste (A & B compound Elteck corp india) Other terminal is pasted with the body of the header the epoxy contact is cured in oven at 80C for 45mins for proper strength of the bonding A cap is put onto the header for protection against mechanical damage

3 2 2 INSTRUMENTAL DETAILS

Inorder to achieve steady state and controlled low temperature a dipstick type conical shaped aluminium cryostat is used the packaged sample is kept inside the cylindrical aluminium chamber filled with oil for good isotropic themal contact and stability as in Fig(3 1) A heater wire of is connected to it for for raising the temperature of the sample up to 330K Power supply to the heater is given by model 3161 30V 150W source A copper constantene thermocouple refe ence junction is kept in ice water mixture (273K) other junction is kept close to the sample (TO5 header) The thermocouple is fed toa GPIB controlled keithley digital multimeter (Model 196) and hence the temperature is monitored A boonton capacitance meter (Model 72B) with 50μm response time operated at 1mHz is used for capacitance measurements Programmable voltage is generated with

the help of a plug in AD/DA card(Model PCL 718) The applied voltage and capacitance meter analog output are digitalized through two input channels of keithley high speed voltmeter (K194A) which can store 64KB data For a typical C-V measurement at the required temperature the voltmeter is trigerred internally to measure the applied voltage and the capacitance of the sample simultaneously The contact is done through IEEE 488 interface bus The data is transfered from internal buffers of the high speed voltmeter to the computer for further processing The whole set up is computer controlled one except for the temperature

3 3 EXPERIMENTAL DETAILS

A semiconductor device can be electrically / optically characterized But electrical characterization methods are generally preffered over the optical methods And among the electrical methods C V technique is most commonly used

3 3 1 CAPACITANCE VOLTAGE CHARACTERISTICS

Under this experiment the sample is kept under reverse bias and a desired temperature is achieved through proper control of the heater current in the the cryostat and the liquid nitrogen level The bias voltage is changed from high to low value and the corresponding capacitance is monitored through two input channels of keithley high speed voltmeter (K 194A) The control is done through IEEE 418 interface bus THE data is transferred from internal buffers of the high speed voltmeter to the computer for further processing

3 3 2 CAPACITANCE TRANSIENT CHARECTERISTICS

The device under test is kept under desired reverse bias to ensure emptying of traps above fermi level in the depletion region The required temperature is achieved through proper control of the heater current and liquid nitrogen level Filling pulses and trigger pulses (foer synchronous purposes) are generated from PCL 718 card along with the help of a multiplexer as in Fig(3 2) Filling pulse is applied leading to partial or complete occupancy of traps in the depletion region Inorder to get capacitance transients the analog output of the capacitance meter is digitalized using high speed voltmeter keithley 194A with 16 bit accuracy The experimental setup is as in Fig(3 3)

3 3 3 THERMALLY STIMULATED CAPACITANCE MEASUREMENTS

TSCAP measurement was originally used for insulator and latter adapted to lower resistivity semiconductor when it was recognized that reverse biased SCR is a region of high resistance During the measurement the device is cooled at reverse bias and the traps are hence get filled up at the end of the cooling with majority carriers at zero bias Then the device is reverse biased heated at almost constant heating rate The steady state capacitance is measured as a function of temperature Capacitance steps are observed in the TSCAP spectra as traps emit their carriers By appling either the device reverse bias/zero bias and foward bias filling pulse or the diode is applied with forward bias then this is called forward bias tscap

3 3 4 DEEP LEVEL TRANSIENT SPECTROSCOPY

DLTS signal is basically the digitalized c t wave form at each temperature during whole temperature scan from 80K 330K In DLTS measurement the device is cooled under reverse bias till the required temperature (~80K) is ahieved During the heating cycle a filling pulse of 50msec is applied and at each temperature typically ten transients are taken and averaged which improves the signal to noise ratio is dramatically Typically DLTS signal corresponding to seven different rate windows are stored in a single temperature scan in order to obtain arrhenius plot If the whole experiment is carried out at foward bias then it is called forward bias dlts The schematic diagram of DLTS measurement system is given in fig(3 3)

3 3 TIME ANALYSED TRANSIENT SPECTROSCOPY MEASUREMENT(TATS)

This is another technique besides DLTS for characterising trap parameters In this measurement at stabilized temperature the entire transient c t is acquired with 30 000 data

points and data in logarithmic time is extracted after proper filtering For obtaining arrhenius plot transients at several temperature are taken The schematic diagram of the experimental setup is exactly the same as DLTS setup(Fig 3 3)

CHAPTER 4

RESULT AND DISCUSSION

4.1 INTRODUCTION

Our main experimental objective is to be able to carry out comparision of electrical characterization results of a set each of n and p type samples prepared under controlled conditions It is helpful to recall at the outset what these preparation conditions are for each sets here though samples have been described in the last chapters The combinations arise from whether ECR hydrogenation is carried out or not and in addition whether the method furnace annealing or RTA Hence for each set the combinations is as follows

	ECR HYDROGENATION	ANNEALING
1	YES	NO
2	YES	FURNACE
3	YES	RTA
4	NO	FURNACE

We first present results for n type schottky diodes and then p type The experiments include C V characterization at different temperatures TSCAP DLTS and TATS on each set

4.2 C-V CHARACTERIZATION OF N-TYPE SAMPLES

A standard method of obtaining information from C V characteristics of a schottky diode involves plotting $1/C^2$ vs V from which the capacitance yields the value of the edge of the depletion layers and carrier concentration is obtained from the slope $d(1/C^2)/d(V)$ at that distance The voltage axis intercept indicates the built in voltage if the

doping concentration is uniform in the region of the sample under scanned We use this method profitably to compare the effects of processing conditions which have their most dramatic effect in the near surface region of the sample

Fig 4 1 shows the $1/C^2$ vs V plot for the sample not hydrogenated (no hydrogenation + Furnace Anneal) but furnace annealed at 500C for 30 min The plots are typical of normal schottky diodes with V_{bi} changing within 0 86 to 0 56 Volts The built-in potential depends on a variety of interface conditions through barrier height and doping levels of the semiconductor Instead of discussing in detail we would like to take it as an indicator of the interface quality in terms of damage We will postpone the discussion of profile information for the time being

Compare now similar plots given in fig 4 2 ECR hydrogenation but without any annealing(ECR+NO Anneal) Clearly V_b is now much larger indicating modification of the near surface of the layer The next figure Fig 4 3 shows similar plots after RTA annealing which brings the characteristics closer to the unhydrogenated sample The efficacy of undoing the damage caused by ECR is demonstrated However samples that were furnace annealed (at the same temperature as RTA) but for 10 minutes (instead 5 secs in RTA) has a different story to tell as in Fig 4 4 The built in voltages are now unrealistically large varying between 6 to 30 Volts This we take as the signal that validity of simple Schottky structure is to be questioned and large amount of interface traps or formation of an insulating layer must be responsible for the unusual behavior Apart from this sample for the other three the comparisons of C V at low temperatures are shown in Fig 4 5 The temperature are not exactly the same for each but that is inconsequential for the qualitative inference that we want to get from it Note that (ECR+RTA) sample has close characteristics to just FA sample whereas ECR processed sample without annealing shows the presence of large amount of interface charge and damage The slight variation of slope and V_{bi} between the (ECR+RTA)sample and the (No ECR+FA) sample can be attributed to deactivation of dopants in the case of (ECR+RTA) sample due to hydrogenation

The zero bias width of space charge layer also provide similar indications More the damage or interface charge larger is the width reaching very large values for ECR+FA samples Typical widths that could be profiled through measurement at both room temperature and at low temperature are tabulated in Table 4 1 Note that it is not possible to obtain information less than a micron which would have been most affected by any deactivation due to hydrogenation The fact that for each sample the width is larger as the sample is cooled is typical of most schottky samples and is principally due to among other things deionization of dopants

In the ECR+FA samples the depth profile at room temperature is shown from 9μm to 13μm in Fig 4 6 It appears that there has been severe hydrogenation effects deep in the sample reducing the doping concentration Since we are able to measure it only at large distances it is difficult to pinpoint a mechanism responsible for decreasing doping concentration at large distances A possible explanation may be migration and complexion of defects during furnace annealing In contrast RTA annealing being for much shorter periods does not lead to such effects

4 3 TSCAP OF N-TYPE SAMPLES

Fig 4 7 shows normalized thermally stimulated capacitance curves between 90 300K for all the four samples The unusually large temperature dependence of (ECR+FA) sample again stands out in contrast This further reinforces the idea that complexetion and defect formation leading to the deactivation of dopants has its ionization energy much larger than standard p type dopants The TSCAP plots for the other three cases are shown in fig 4 8

In none of the plots we find any thermally activated process corresponding to release of carriers from traps Hence the plots can actually be treated as temperature dependence reverse bias capacitance at 4 5V

4 4 DLTS STUDIES ON N- TYPE SAMPLES

All the above four types of samples were used for DLTS studies to obtain information on possible occurrence of deep level traps Similar set of samples were used almost a year ago elsewhere[23] to show that many deep levels arise after ECR processed samples are annealed This study has primarily been geared towards thorough study of the nature of these deep levels However except for one sample none others showed any trace of deep levels to a sensitivity of 0 001 times the background which was estimated 1×10^{15} cm^{3} Hence no more than $10^{12}cm^{3}$ concentration was detected

Curiously ECR hydrogenated samples which also underwent furnace annealing showed occurrence of a major minority carrier peak corresponding to a hole trap Fig 4 9 shows a typical normalized DLTS plot for three different rate windows In order to check the exponential parameters The line passing through the exponential signal are the simulated curves Note that the exponential curves are broader than the simulated curves and specially notable for the case of rate window 4 33 msec with peak near 250K The broadening is unmistakable inspite of the presence of noise It is probably appropriate to add here that the noise is two three fold larger in this case than a typical spectrum with similar sensitivity We attribute this to the fact that in this case we are dealing with a nearly intrinsic material which is prone to picking up electromagnetic interference more than usual metal semiconductor diode The level of concentration is estimated from $\Delta C/C$ height calculation is about $10^{10}cm^{3}$ close to intrinsic carrier concentration of silicon at room temperature

The emission time constants as a function of temperature are analyzed as in an Arrehenius plot by plotting $\ln(\tau T^{2})$ as a function of 1000/T Fig 4 10 shows such an Arrehenius plot The slope gives the activation energy to be 0 386ev and the capture cross section obtained from the intercept is $3\ 2\times10^{16}$ cm^{2} However the value of capture cross section is not so reliable since slight variation in the fitted line can make a large deviation to the intercept in such a plot

4 5 TATS ANALYSIS OF MINORTY CARRIER TRAP

Since broadening is observed in DLTS line shape the transients must be non exponential However calculation of activation energy from Arrehenius plot is known to be a robust against broadening in DLTS line shape if it is due to distribution in energy of the trap Chief cause of non exponentiality of transients are

(i) large concentration of trap(i e comparable to back ground doping)

(ii) distribution in energy of the trap or occurrence of multiple traps and (iii) significant series resistance in the device

In the present case the height of DLTS peak is too small ($\Delta C/C \sim 0\ 001$) Hence large concentration is not the cause To be able to distinguish between other two reasons we perform time analysed transient spectroscopy (TATS) Since TATS is an isothermal technique equivalent to DLTS processing of the signal [36] any temperature dependence in line shape can be ruled out Further it has been shown that in DLTS the natural width of the DLTS peaks depends on the choice of rate window and the trap energy[36] Hence a more reliable study of line shape is possible through TATS

Fig 4 11 shows typical TATS spectra for three different temperatures along with simulated spectra Though signal to noise ratio is poorer in this case lineshape is quite close to signal one would expect from exponential transients This shows that the line broadening observed in case of DLTS was not due to any distribution of emission constants Most likely reason then appears to be change of series resistance with temperature In fact recall that strong temperature dependence in capacitance has been presented in Fig 4 4 for this sample Further the sample carrier concentration is quite low and hence it is likely that temperature dependence of series resistance is playing a role in making the transients non exponential

The Arrhenius plot for the same trap as would be obtained from TATS analysis also shown in Fig4 10 The activation energy obtained is 0 32ev and the capture cross section $2\ 6\times10^{17}$ cm^2 from least square fitting of the points A comparision of the plot with that of DLTS also shown in the same figure shows that there are systematic differences between DLTS and TATS A comparision of energy and capture crosssection

obtained from the two methods are shown in table 4 2 The scattering of points around the TATS fitted line is more for TATS probably due to poorer signal to noise ratio However as is clear from the the preceding discussion on lineshape analysis of DLTS TATS data is more reliable Hence we would conclude that the observed minority carrier is (E_V +0 6)ev in the n type sample subjected to ECR hydrogenation followed by furnace annealing

4 6 ORIGIN OF THE MINORITY CARRIER TRAP

All the samples studied in this work are Schottky diodes and therefore supply of minority carrier is not excepted to fill up the traps Hence it is surprising that one observes a hole trap for a metal semiconductor contact on n type However since we have observed cosiderable deactivation of dopants bordering on making the sample highly resistive it looks plausible that the band bending at the interface is no longer as simple as that of a metal semiconductor contact It is well known that contact to semi insulating materials can inject both type of carriers into the active layer Since the carrier concentration is 10^{12} cm^{3} it is the most likely mechanism There is also possibility that the layer suffering the most damage at the interface due to ECR treatment turns p type on long furnace annealing due to larger carrier removal by defect complexation In that case the structure would have a p n junction imbedded near the subsurface region abd would be able to inject holes needed to populate minority carrier traps To distinguish between the two possibilities more systematic studies than can be accommodated in the scope of this work are needed

The fact that TATS lineshapes corresponded to nearly exponential transients at different temperatures the trap appears to be due to a well behaved point defect inspite of the fact that the DLTS lineshapes were broadened Hence the origin of this trap does not lie in electrical activity of any extended defects themselves However point defects decorating extended defects as dislocations can t be ruled out Presence of extended defects is to be suspected in this sample Since it is known that they are formed upon annealing after creation of damage(specially implantation induced damage) The dislocation formation in silicon is favoured at these low temperatures of furnace annealing and they themselves can be annealed out only after heat treatment of the samples beyond 900 C

Moreover the traps have been observed in DLTS and TATS in quite deep regions of the sample where ECR damage is supposed to have been created at the surface It is likely that furnace annealing induces threading dislocations to penetrate deep into the sample Also since defects such as vacancy and interstitials migrate large distances in silicon at relatively low temperatures Therefore it is possible that large hydrogen clusters or some more complex intrinsic defect clusters are responsible for both carrier removal and trapping activity in the bulk

During the course of this work we have attempted to compare these results with another set of samples where Mev Ar^+ ions were used to create deep buried damage within a metal semiconductor diode where the semiconductor was a n type We will confine ourselves to only a qualitative comparision of results from such a sample with the result presented above In this particular sample 1 3 MeV Ar was used to create peak damage at a distance of 1 2μm from the surface and than furnace annealed at 400 C A typical DLTS plot is shown in Fig 4 13 for three different rate windows Again note that there is a presence of minority carrier trap though the sample is majority carrier metal semiconductor device There are also present two other majority carriers The trap activation energies are obtained from the Arrehenius plots obtained from DLTS analysis as shown in the fig4 14 Though the activation energy for the minority carrier is different in this case probably because of the nature of damage envioronment the fact that such minority carrier traps appear in damaged layers on removal of carriers in that region is striking They in fact may have common origin in clustering of vacancies or interstitials Hydrogen involvement in the minority carrier trap on this count can be ruled out in our ECR hydrogenated sample It has been shown specially that [35] surface damage can migrate result in a flux of interstitials which can deep into the sample

4 7 RESULTS ON P TYPE SAMPLE SET

We will now present results of similar experiment on the set of p type samples prepared under identical conditions(similar to the n type samples) A typical plot of $1/C^2$ vs V for ECR hydrogenated sample without annealing (ECR + NO anneal) for three different temperatures is shown in Fig 4 15 Note that unusual built-in potential is again an

indicator of a damaged or high resistivity layer in the near surface region Fig 4 16 shows similar characteristics for RTA annealed samples These behave as expected of a normal metal p Si sample meaning RTA has been effective in removing surface damage Unlike in n type sample furnace annealing of ECR treated samples are close in c v characteristics to RTA treated samples Here the phenomena of deactivation at large distances is not observed and there is little difference between RTA and furnace annealing(FA) For purposes of quick comparison $1/C^2$ vs V plots for the three samples are plotted for low temperature in Fig 4 17 The comparison is given for the low temperature since all the plots are very good straight lines indicating uniformity of carrier concentration in the region being scanned

Fig 4 18 (a) & (b) shows comparison of depth profiles obtained from the c v analysis The profiles turn out to be the same in each case for deeper regions The only difference is the that the region of the sample that one is being able to profile is different This is clearly due to the fact that changes at the interface region and within the zero bias depletion width control the width of the space charge length The damage is high due to ECR treated samples alone and it recovers due to annealing by both methods as expected In all these processes effect of deactivation of carriers in the deeper region is not observed This must be confined to surface and sub surface layers only thus modifying the barrier height characteristics

As in the case of n type samples no evidence of steps in TSCAP plots was obtained and hence TSCAP plots as shown in Fig 4 19 only indicate temperature dependence of capacitance in each case The sensitivity of detection for TSCAP was of the order of $10^{13}cm^{3}$ which may not be sufficient to detect deep traps present in the materials Therefore we attempted to detect deep levels using DLTS and TATS as well However the p type samples had larger reverse leakage current and hence the transient spectrometer could not be used in its most sensitive regime making the lowest detectable concentration as $3 \times 10^{12}cm^{3}$ It is significant to note that all the deep levels detected by Nam & Ashok[23] in these materials were in the range of $10^{12}cm^{3}$

4 8 COMPARISON BETWEEN N- & P- TYPE SAMPLE SETS

It is clear from the results presented in this chapter that the behaviour in n and p type have common trends in general but significant specific differences do exist As far as surface damage is concerned in both set of samples it manifests Similarly in both sets ECR hydrogenation alone causes the damage and are effectively removed by RTA annealing A surprising result has been that furnace annealing after ECR leads to severe deactivation in the bulk for n type while for p type it seems to be as effective

A minority carrier trap was observed in n type furnace annealed sample while for p type similarly sensitive investigation could not through increased built in potential and increased zero bias depletion width be carried out for sample limitations

Most surprising aspects of these results is that on similar setof samples Nam and Ashok showed that many point defects appear after annealing following ECR hydrogenation The samples were stored for about a year before carrying out these investigations here During this time lapse it appears that these defects disappeared most probably due to slow relaxation phenomena Hence we conclude that what was being observed was only an intermediate stage of defect reactions involving a slow processes of defect kinetics

CHAPTER 5

CONCLUSION

Since electron cyclotron resonance (ECR) plasma of hydrogen is emerging as a popular processing technique in silicon technology there is a need to study its effect on the electrical properties of the material Such etching techniques requiring low energy ions normally are used in conjunction with a suitable annealing method such as rapid thermal annealing (RTA) and furnace annealing(FA) In this study we examine the effect soch processing steps on electrical manifestation of surface damage hydrogenation and introduction of traps Capacitance based characterization methods such as c v characteristics at different temperature deep level transient spectroscopy(DLTS) thermally stimulated capacitance (TSCAP) technique and time analysed transient spectroscopy (TATS) have been used Metal semiconductor diodes made from material having undergone suitable combination of the processing steps are used for the study Four sets of samples for each type (n & p) are characterised for comparision purposes

The conclusions are briefly itemized below

(i) ECR hydrogenation alone using a remote plasma does create damage in sufficient amount so as to modify the built in potential severly Though no hydrogenation in the bulk is observed the zero bias depletion layer of schottky diode increases a large amount due to carrier removal and interfaces This is true for both n and p type silicon

(ii) Following ECR hydrogenation if the samples are subjected to RTA annealing at 500 C for 5 seconds there is almost complete recovery of the c v characteristics This is found to be true for both p and n type samples

(iii) Following ECR hydrogenation if the furnace annealing at 500 C for 10 min is carried out then there is severe deactivation of dopants for n type silicon even in the bulk The depletion width widens both due to surface damage and carrier removal C V characteristics of Schottky diodes indicate an unusually large built in potential due to modification of the interface In contrast for p type silicon furnace annealing does not lead to such effects and seems to be comparably efficient to RTA

(iv) Except for ECR etched and furnace annealed samples no other sample of n type set showed any trace of deep levels of less than $1\times10^{12}cm^{3}$ This is specifically surprising since this study was carried out to specifically look into the earlier report of an interesting defect kinetics on the similar set of processed samples in which multiple point defects were observed only after annealing was carried out following ECR hydrogenation plasma cleaning steps We conclude that the defects observed then must have relaxed with aging over a time period of more than a year

(v) In ECR cleaned and furnace annealed sample of n type a minority carrier trap was observed with both DLTS and TATS DLTS lineshapes were broadered than that of a exponential transient case and yielded an activation energy of (E_V+0 38)ev Similar analysing using TATS did not show any noticeable broadening and the measure emission signature was slightly different yielding an activation energy 0 32ev

(vi) The broad DLTS lineshape of the minority carrier is attributed to possible temperature dependence of series resistance since the bulk had suffered severe deactivation of dopants The appearance of a minority carriers is due to type conversion in the interface region during furnace annealing Similar phenomena seem to appear in MeV damage created in n-Si after 400 C furnace annealing Though with different emission signatures a predominant minority carrier trap also observed along with two majority carriers in that case The minority carrier trap is attributed to complex point defects arising out of migrating intrinsic defects in silicon from the surface damage during furnace annealing

(vii) No evidence of any deep traps were found in p type samples in the bulk to a concentration of 3×10^{12} cm^{3} In this case because of sample limitations the transient spectrometer was operated with only sensitivity of 0 001 times of background doping

This study gives a starting point for a more detailed characterization of trap kinetics realizing that slow defect kinetics is active even during storage The exact naturate of defect activation and defect deactivation needs to be studied in more detail The mechanism of carrier removal defect introduction and migration and the role of annealing in controlling it need be studied in future

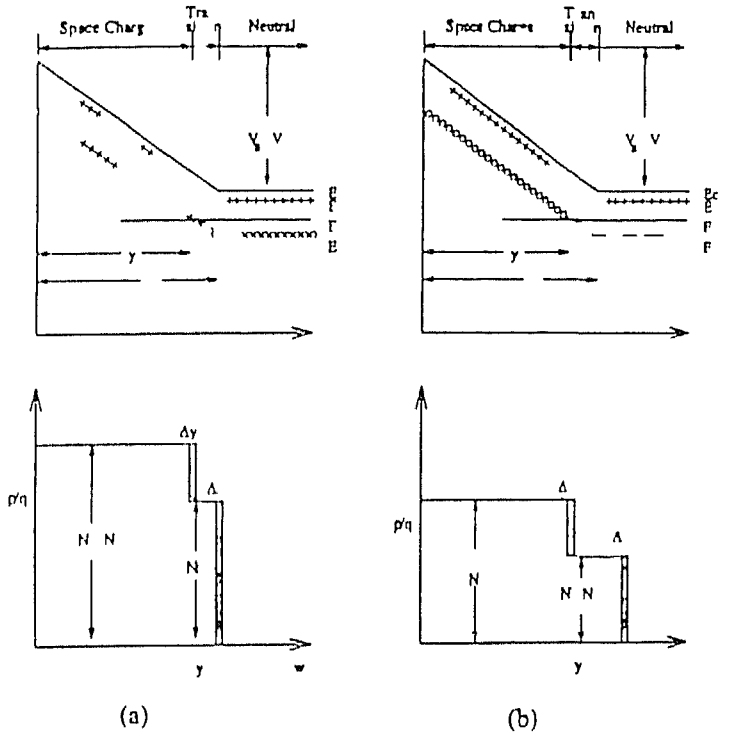

Fig 2 1 Band diagram of a schottky diode under reverse bias with one deep trap V_B is the junction barrier height, V_R is the applied reverse bias E_C is the energy position of the conduction band edge E_D is the shallow donor level E_F is the fermi level, E_T is the trap level Y is the point at which FI and EI intersect and x is the edge of the depletion region Deep donor traps are shown in (a) and deep acceptor traps are shown in(b)

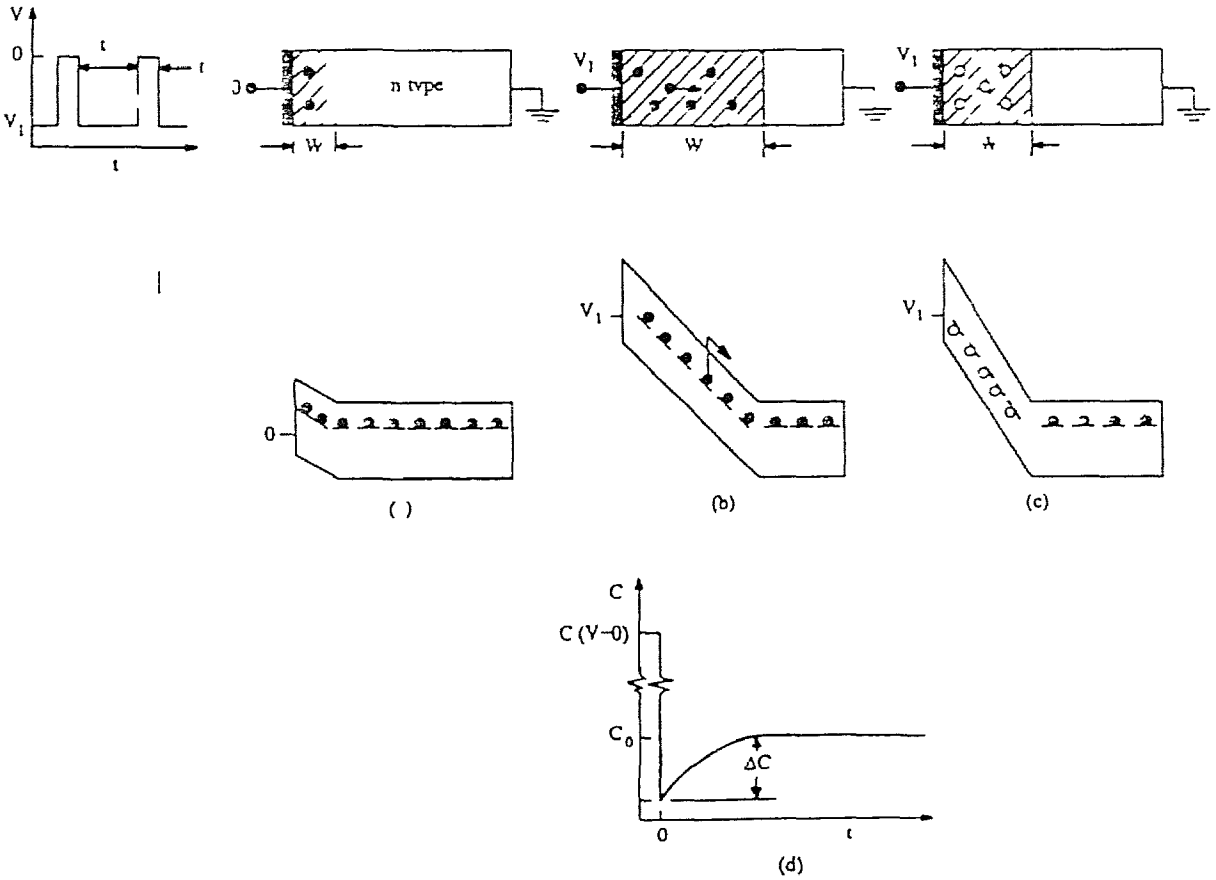

Fig 2 2 A schotkv diode for (a) zero bias (b) reversebias at t=0 (c) reverse bias at t=∞ (d) the capacitance transient

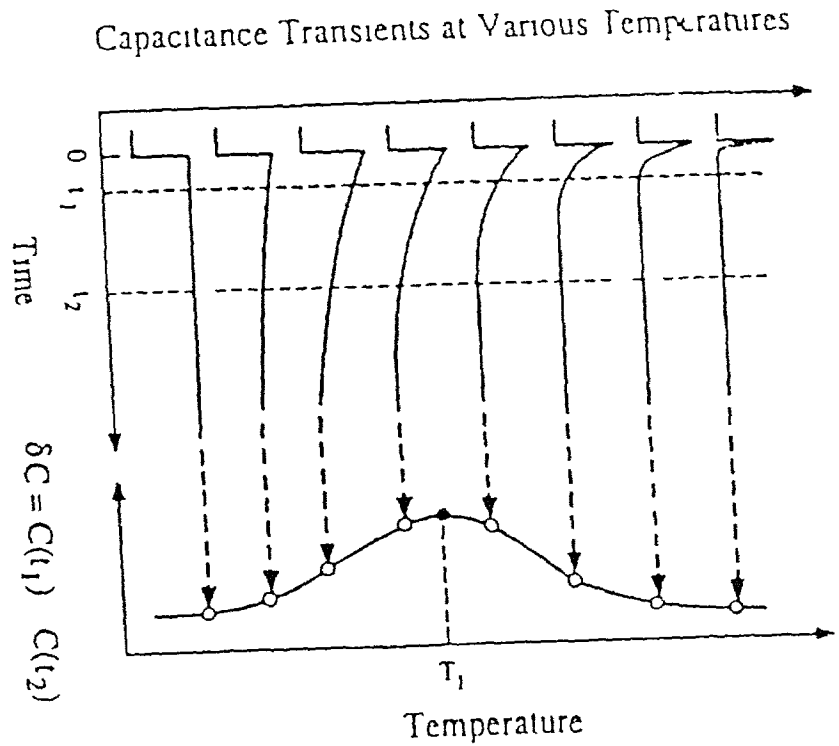

Fig 2 2 Implementation of a rate window by a double boxcar integrator The output is the average difference of the capacitance amplitudes at the sampling times t_1 and t_2

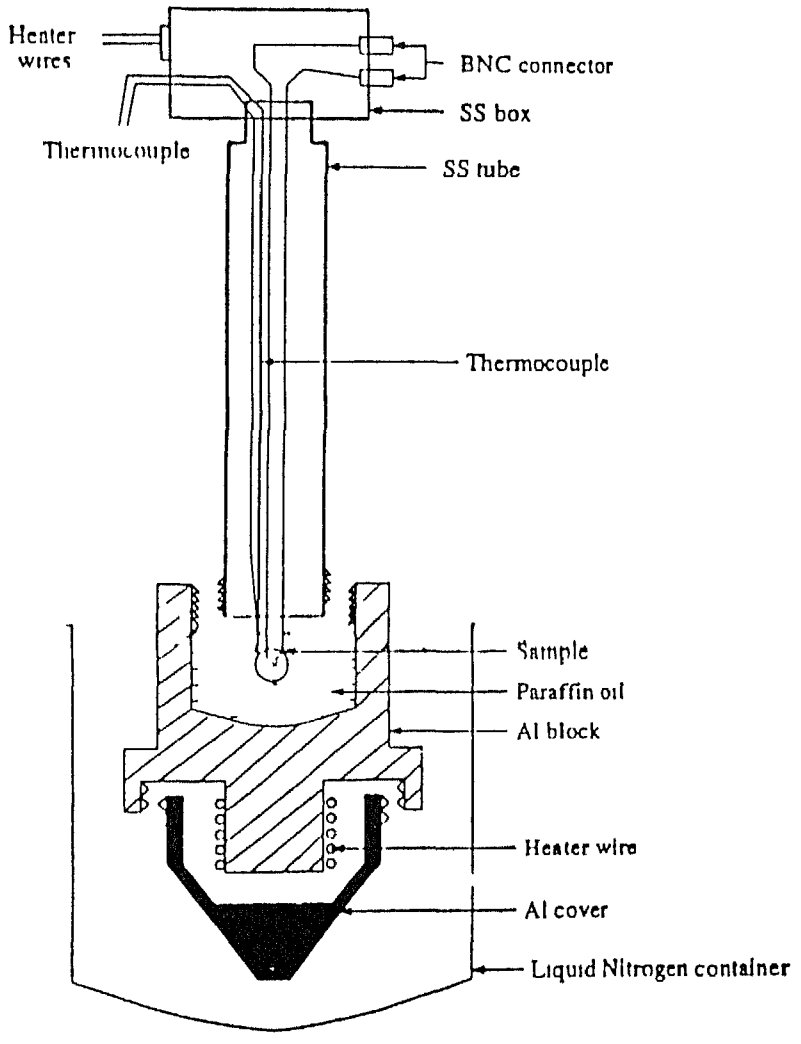

Fig 3 1 Scematic of Cryostat (temperature measurement unit)

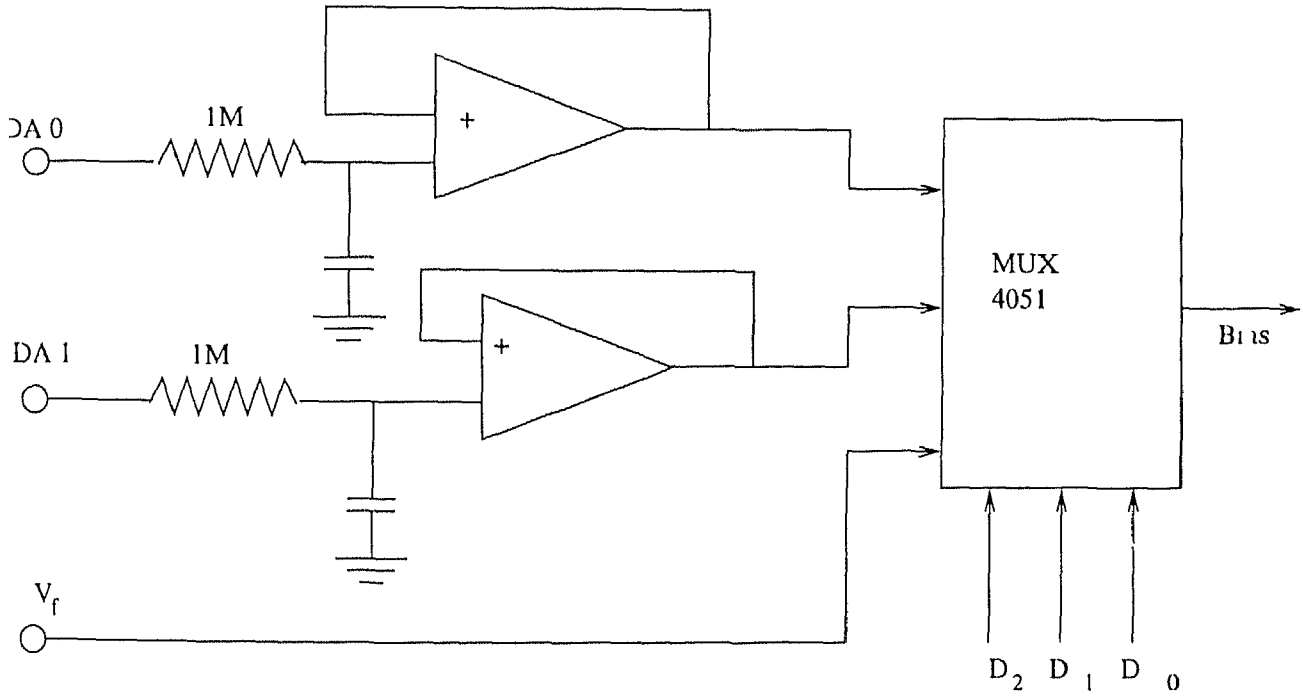

Fig 3.2 Schematic of bias & triggering circuit

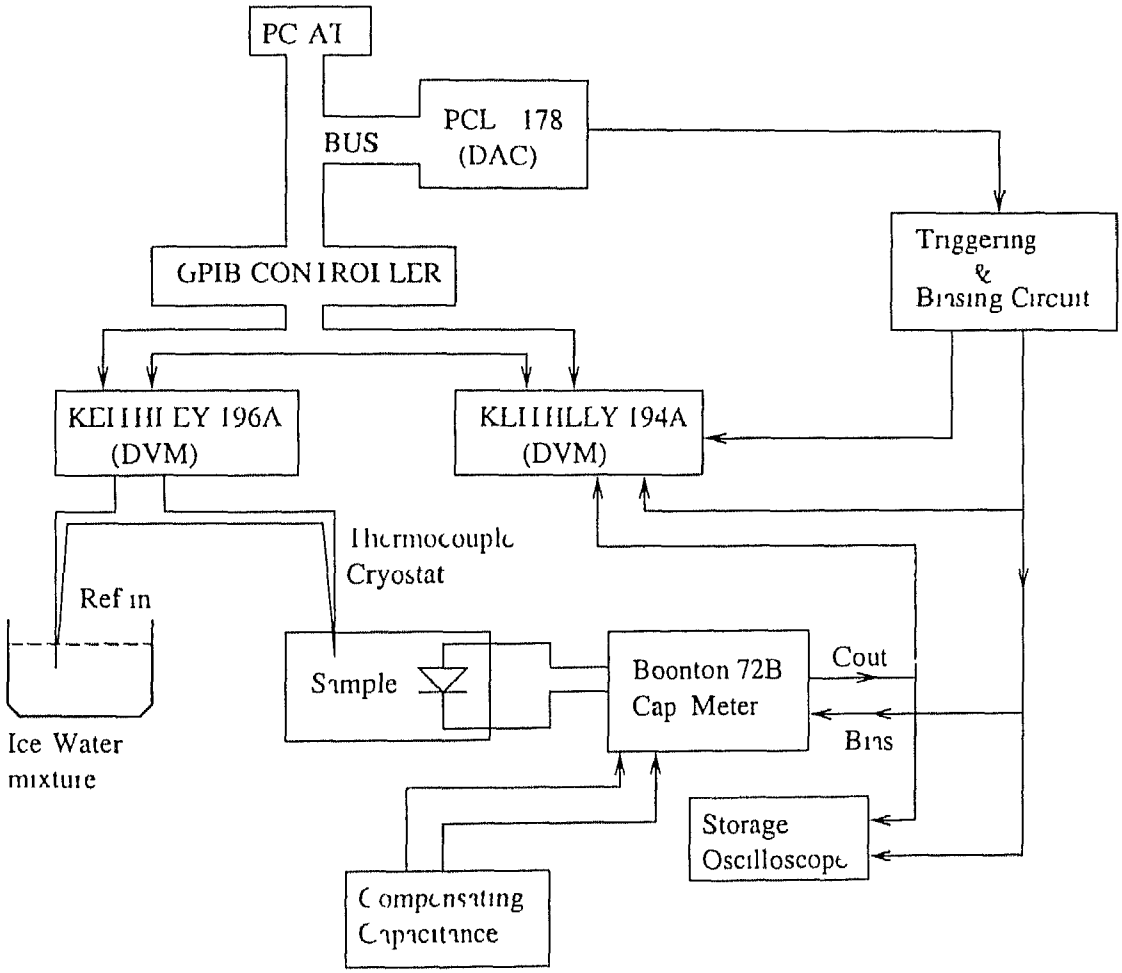

Fig 3 3 Block diagram of capacitance/voltage transient and DLTS/TATS measurement system

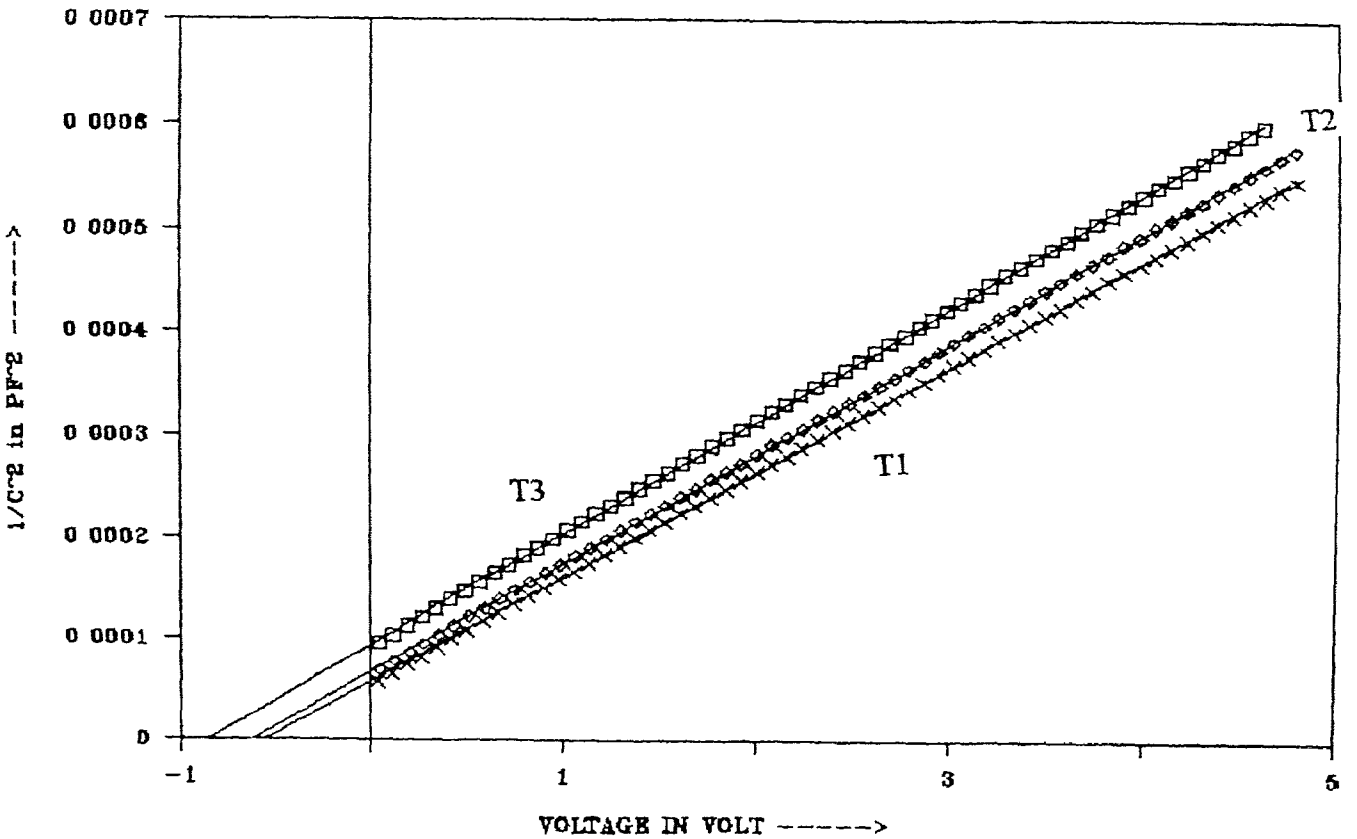

Fig 4 1 Typical C-V characteristics of furnace annealed & no hydrogenated n-Si schottky diode measured at temperatured (T1) 291 66 K (T2) 245 31 K and (T3) 99 48 K

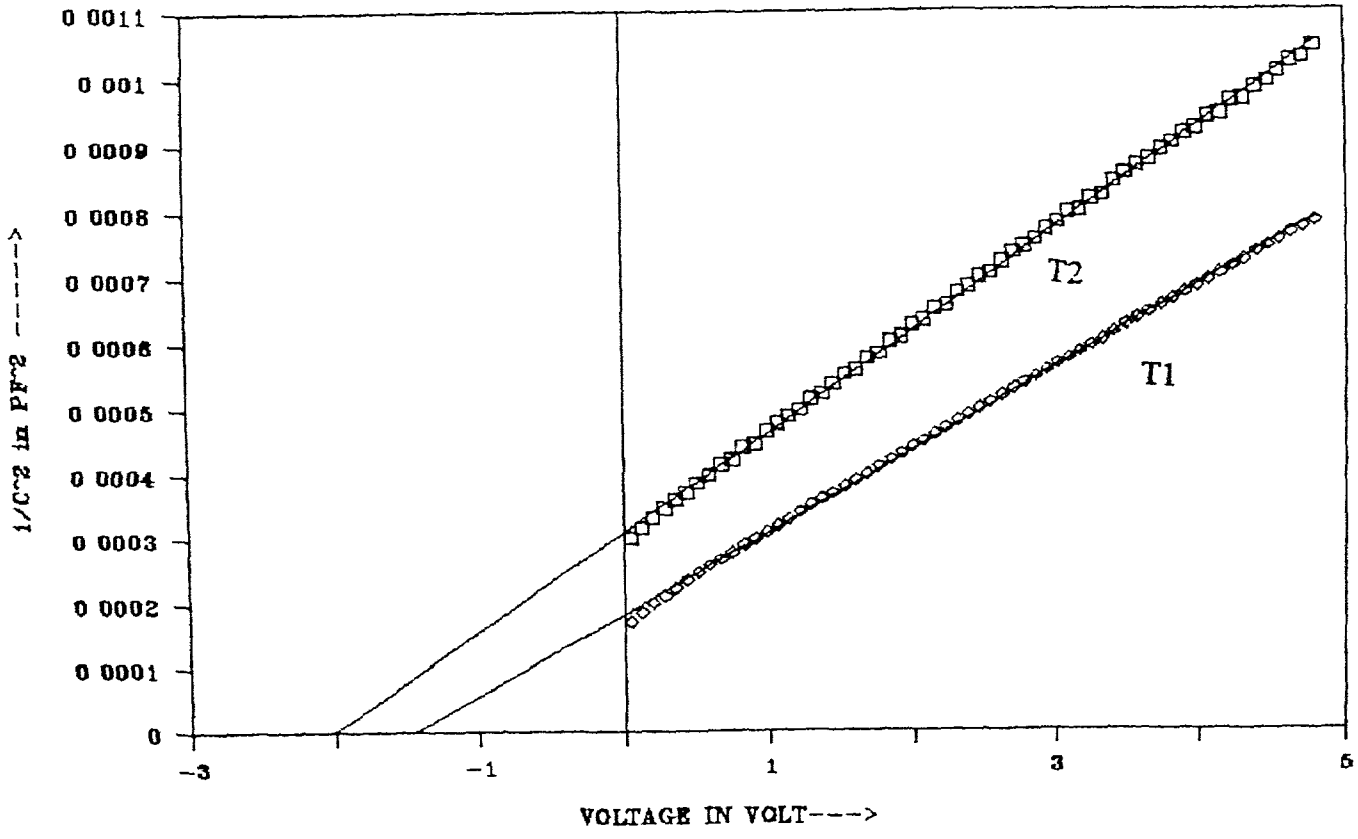

Fig 4 2 Typical C-V characteristics of no anneal & ECR hydrogenated n-type schottky diode measured at temperature (T1) 255 91 K (T2) 107 37 K

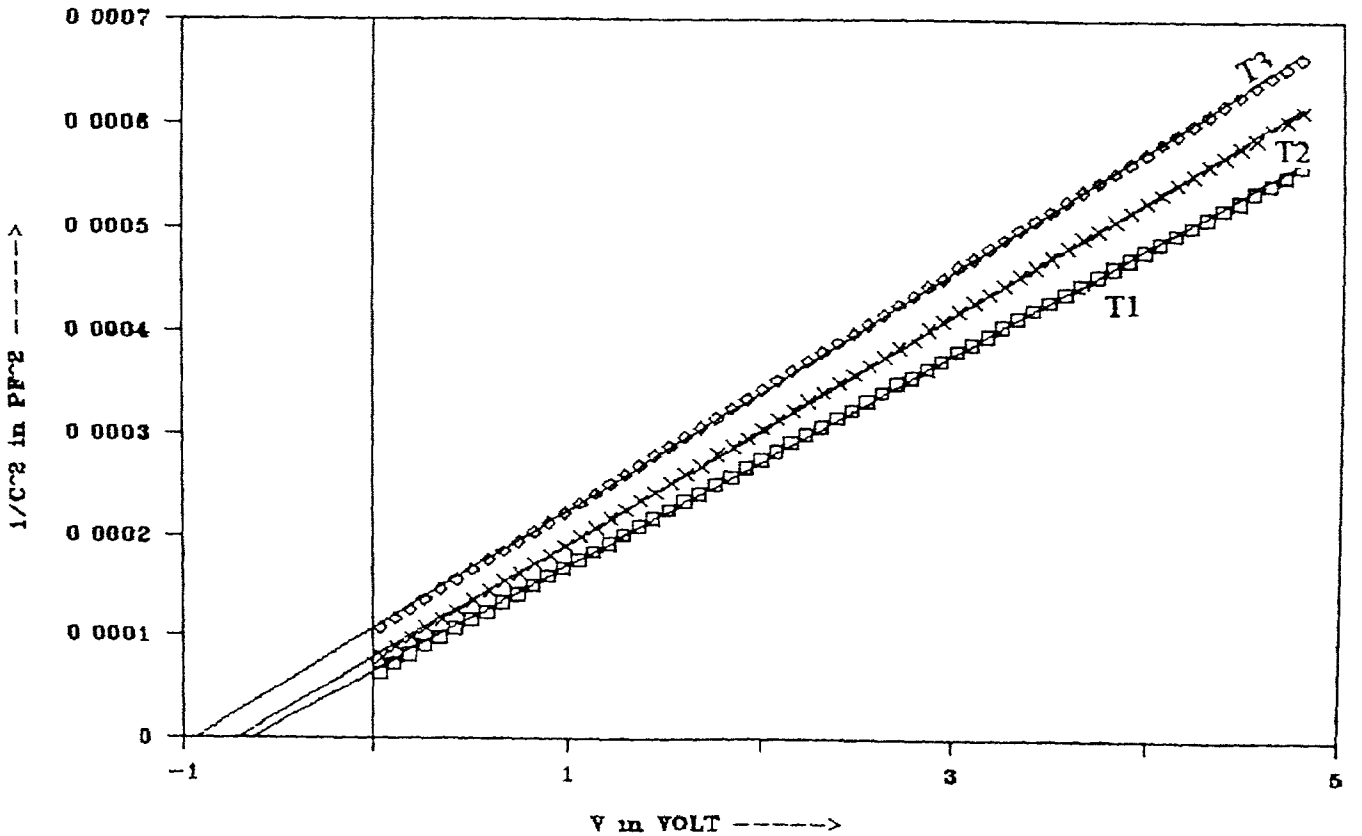

Fig 4 3 Typical C-V characteristics of RTA anneal & ECR hydrogenateded n-type schottky device measured at temperature (T1) 292 1 K (T2) 247 75 K and (T3) 101 54 K

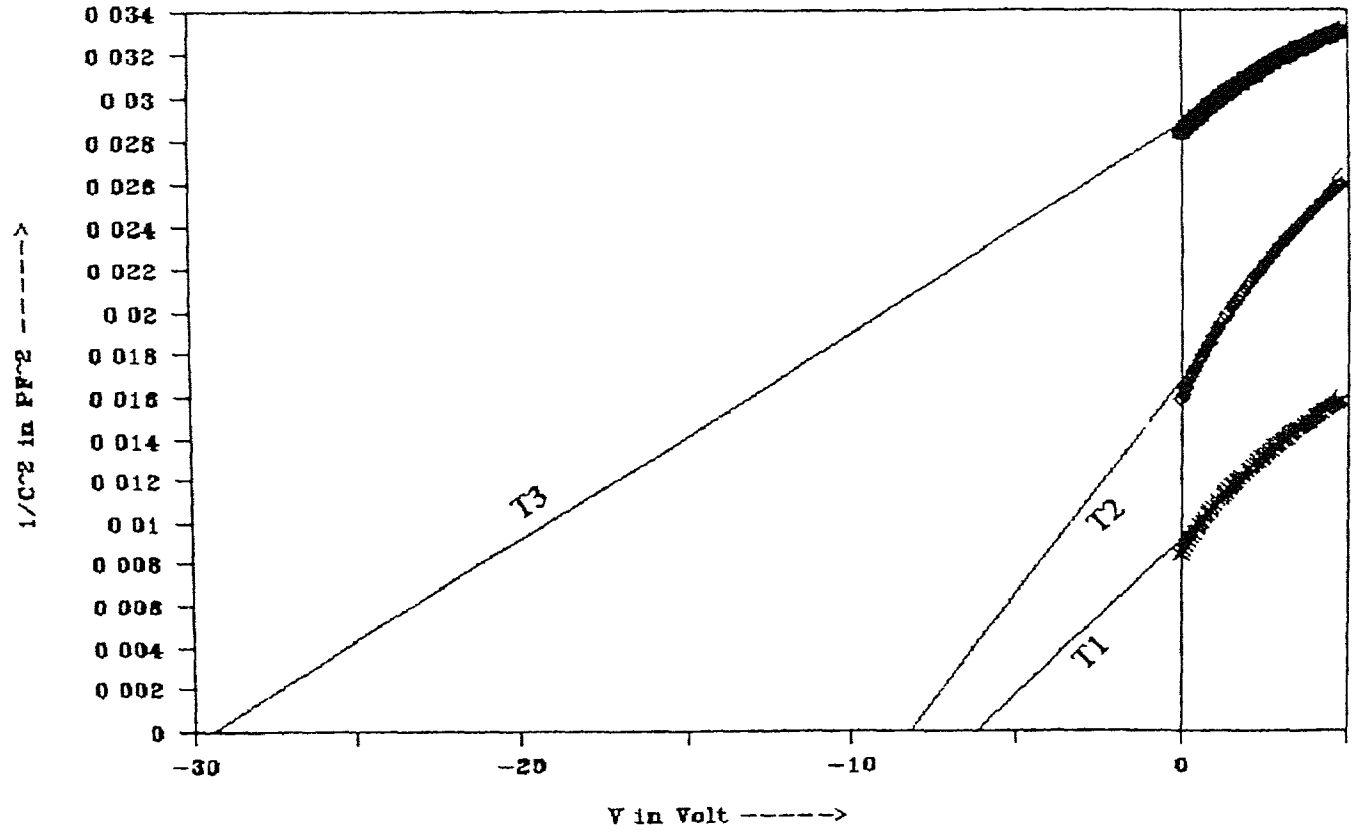

Fig 4 4 Typical C-V charecteristics of furnace anneal and ECR hydrogenated n-Si schottky device measured at temperature (T1) 299 67 K (T2)225 97 K (T3) 93 89 K

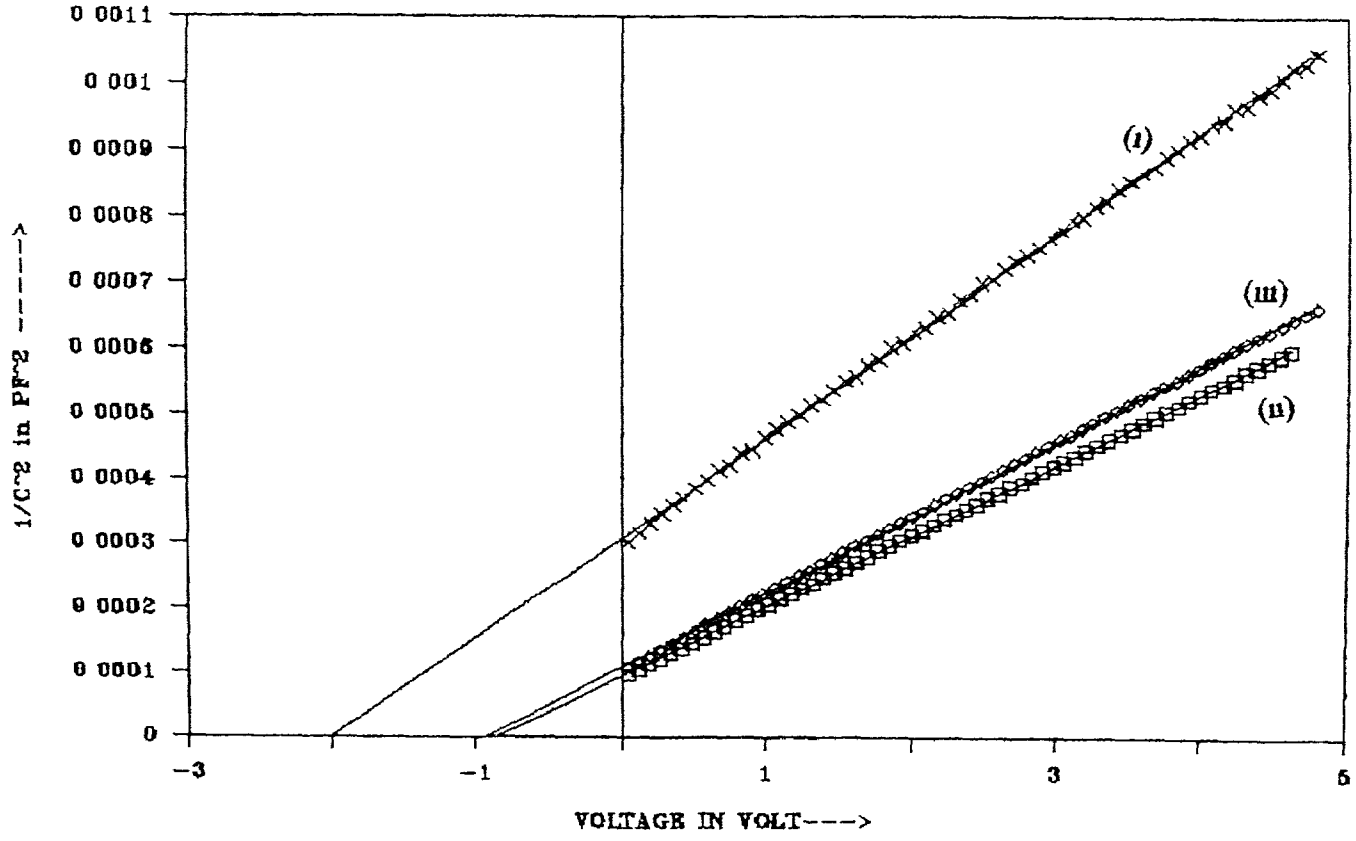

Fig 4 5 Comparision of low temp C-V charecteristics of (i) ECR hyd +No anneal (ii) No hyd +Furnace anneal and (iii)ECR hyd +RTA anneal n Si

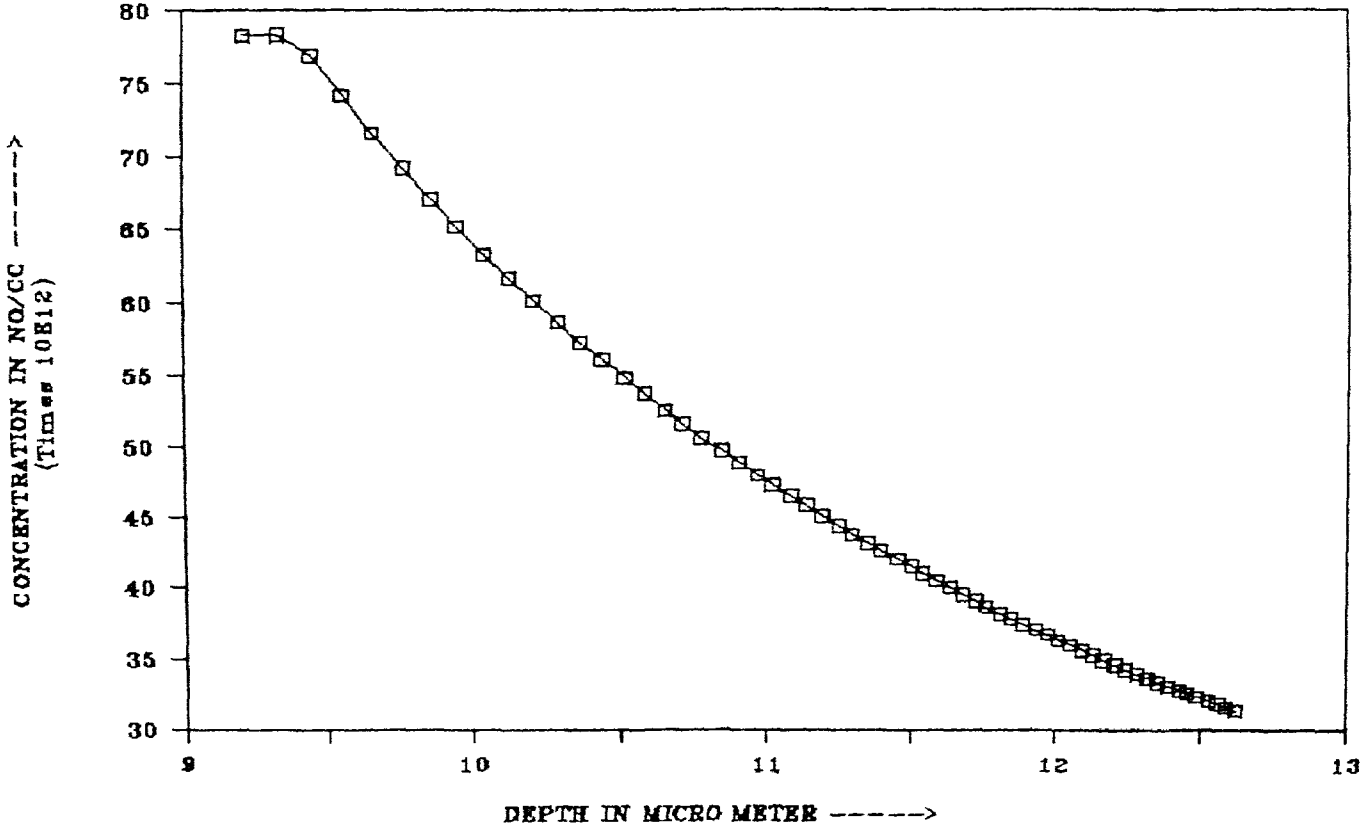

Fig 4 6 Depth profile of Furnace anneal & ECR hydrogenated n-Si schottky device at room temperature

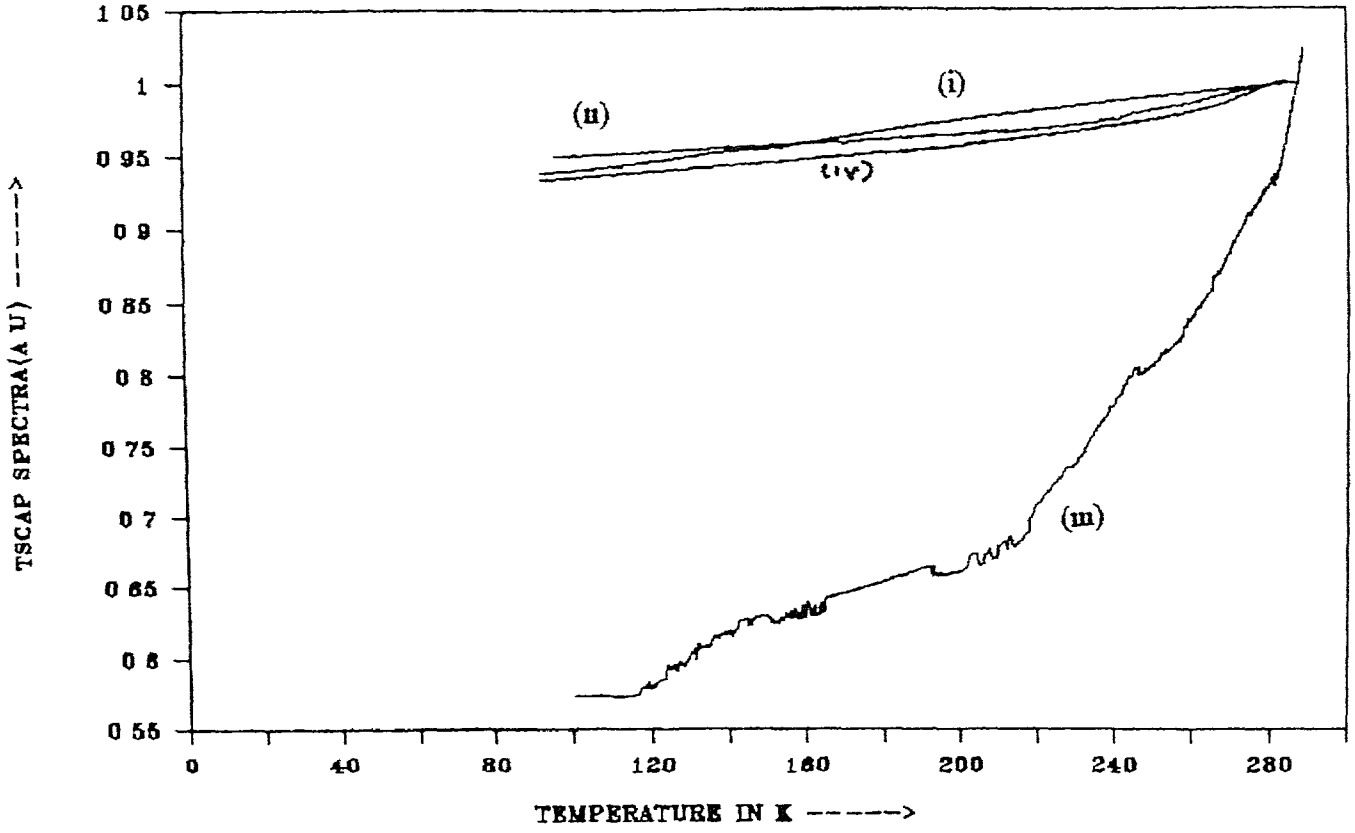

Fig 4 7 Coparision of TSCAP spectra for diff n-Si schottky devices

(i) ECR + NO ANNEAL

(ii) NO ECR + FA

(iii) ECR + FA

(iv) ECR + RTA

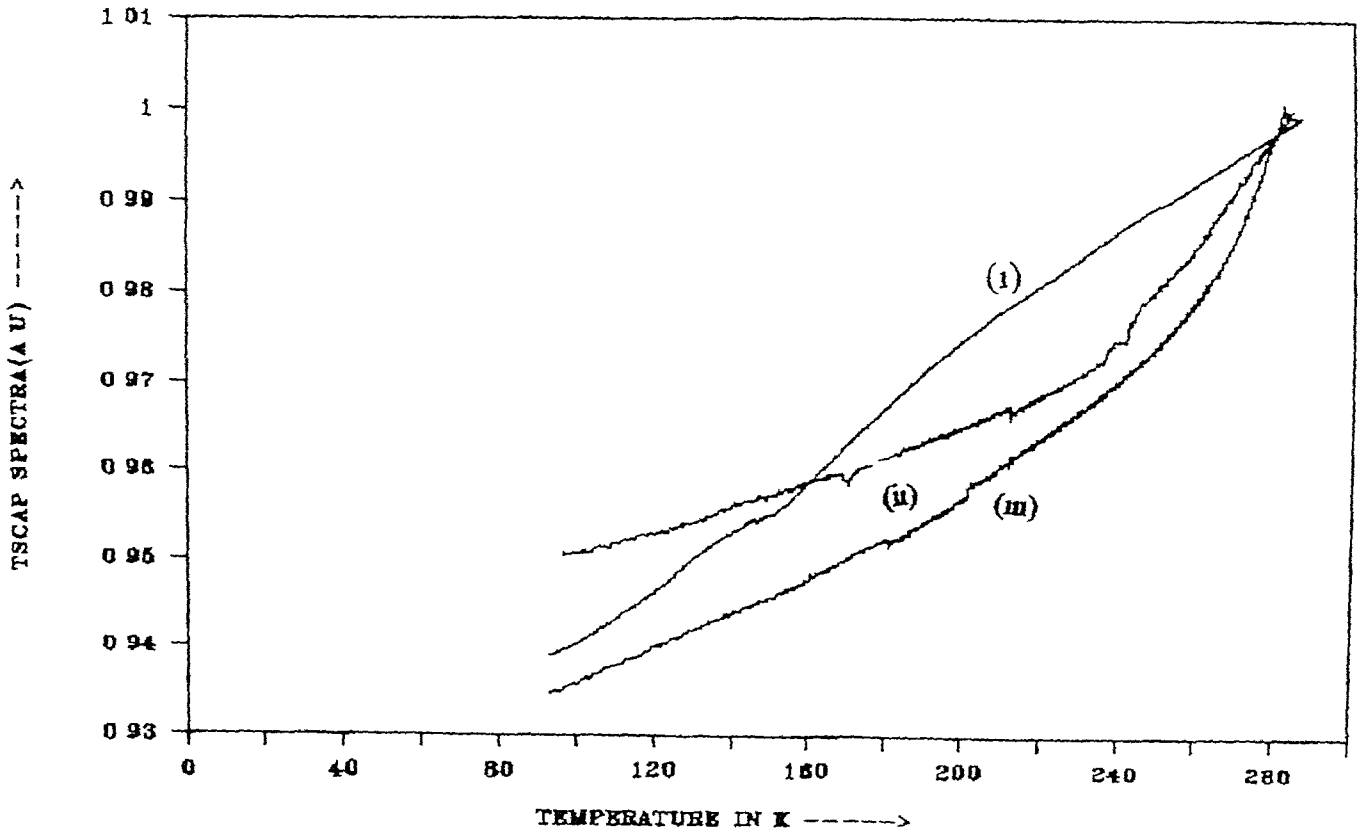

Fig 4 8 TSCAP spectra for (i) ECR hyd +No anneal (ii) No hyd +Furnace anneal and (iii) ECR hyd +RTA anneal n-Si schottky devices

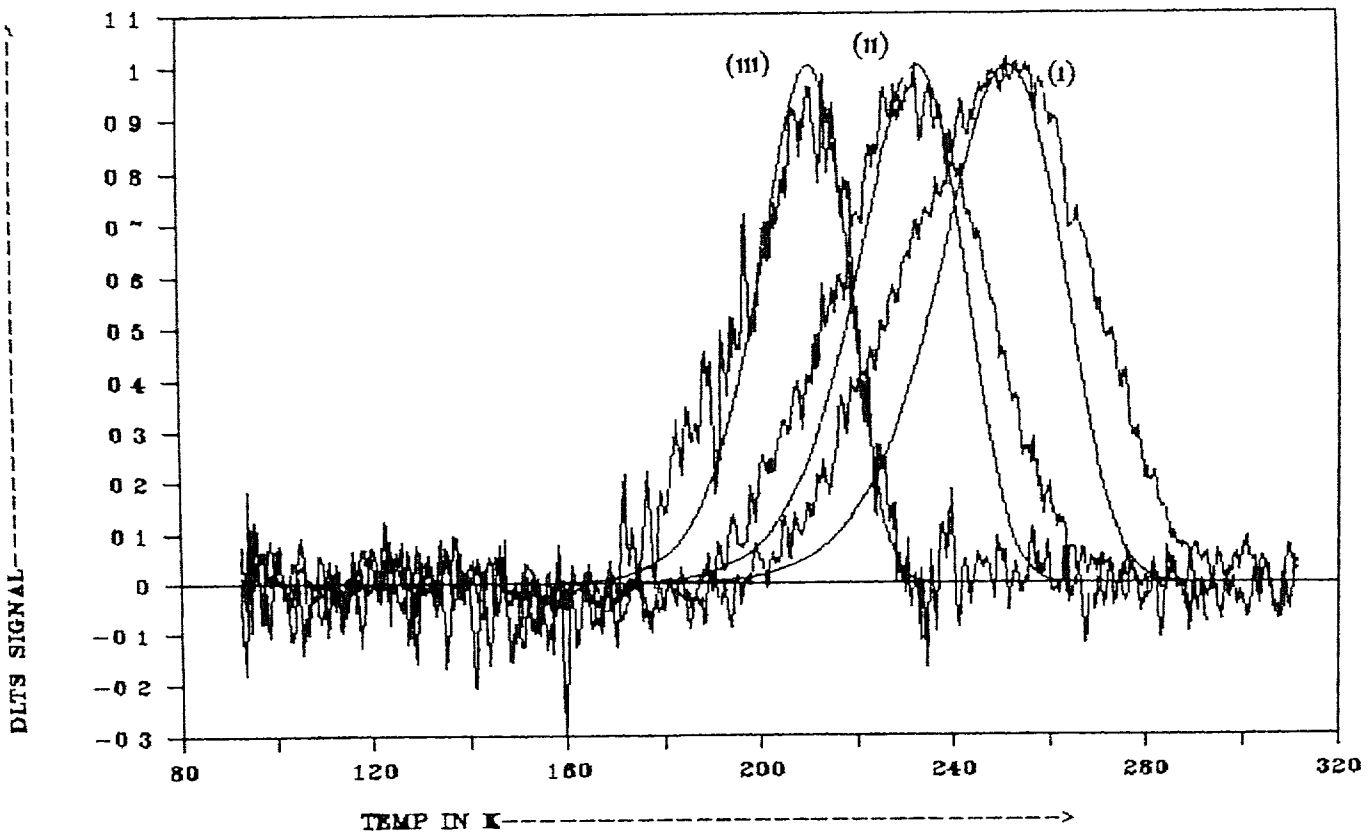

Fig 4 9 Typical DLTS spectra of ECR hydrogenation + FA n-Si schottky device for different rate windows (i) 4 33 ms (ii) 15 85 ms (iii) 200 ms

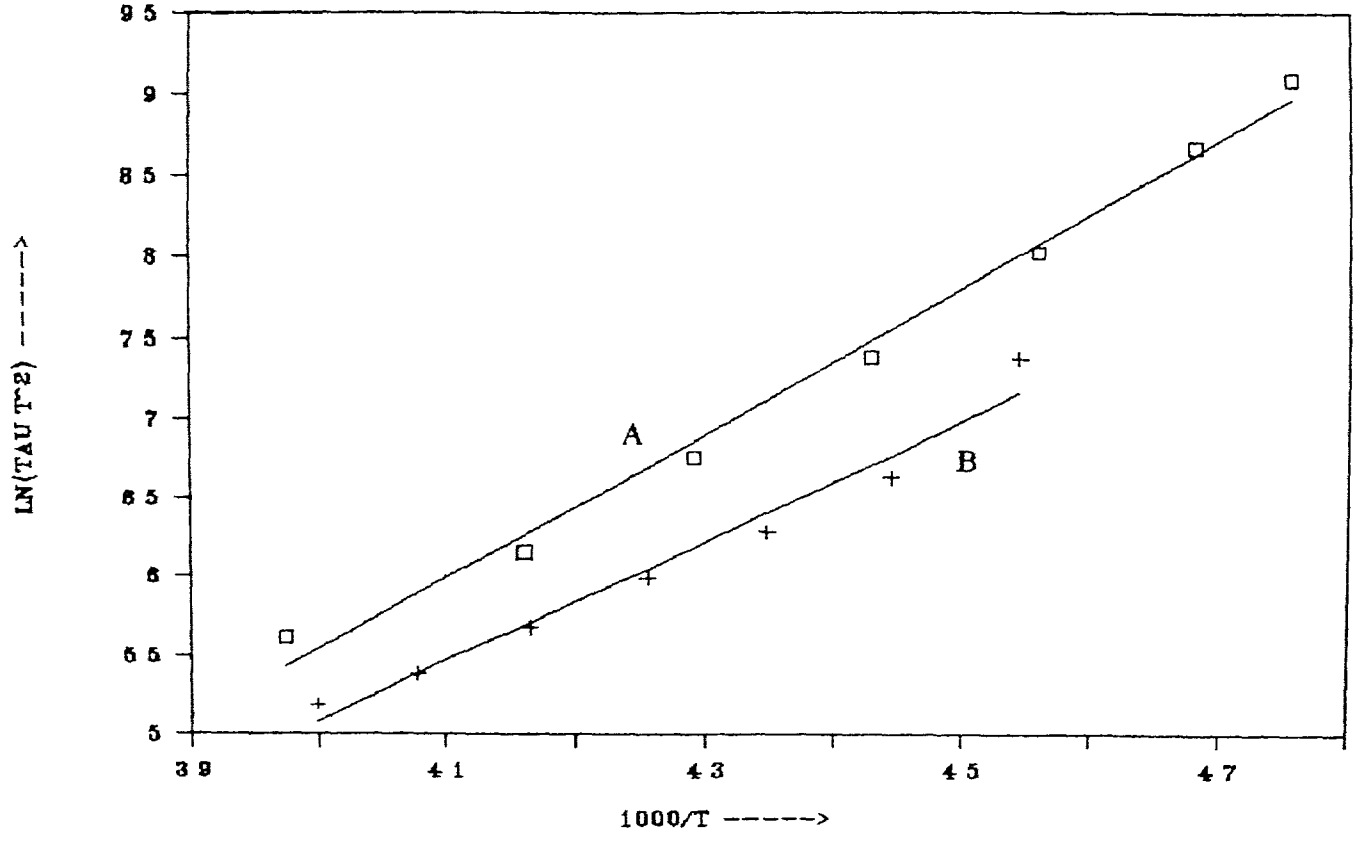

Fig 4 10 Arrhenius plot for ECR hydrogenation + FA n-Si schottky device by DLTS signal(A) and by TATS signal(B)

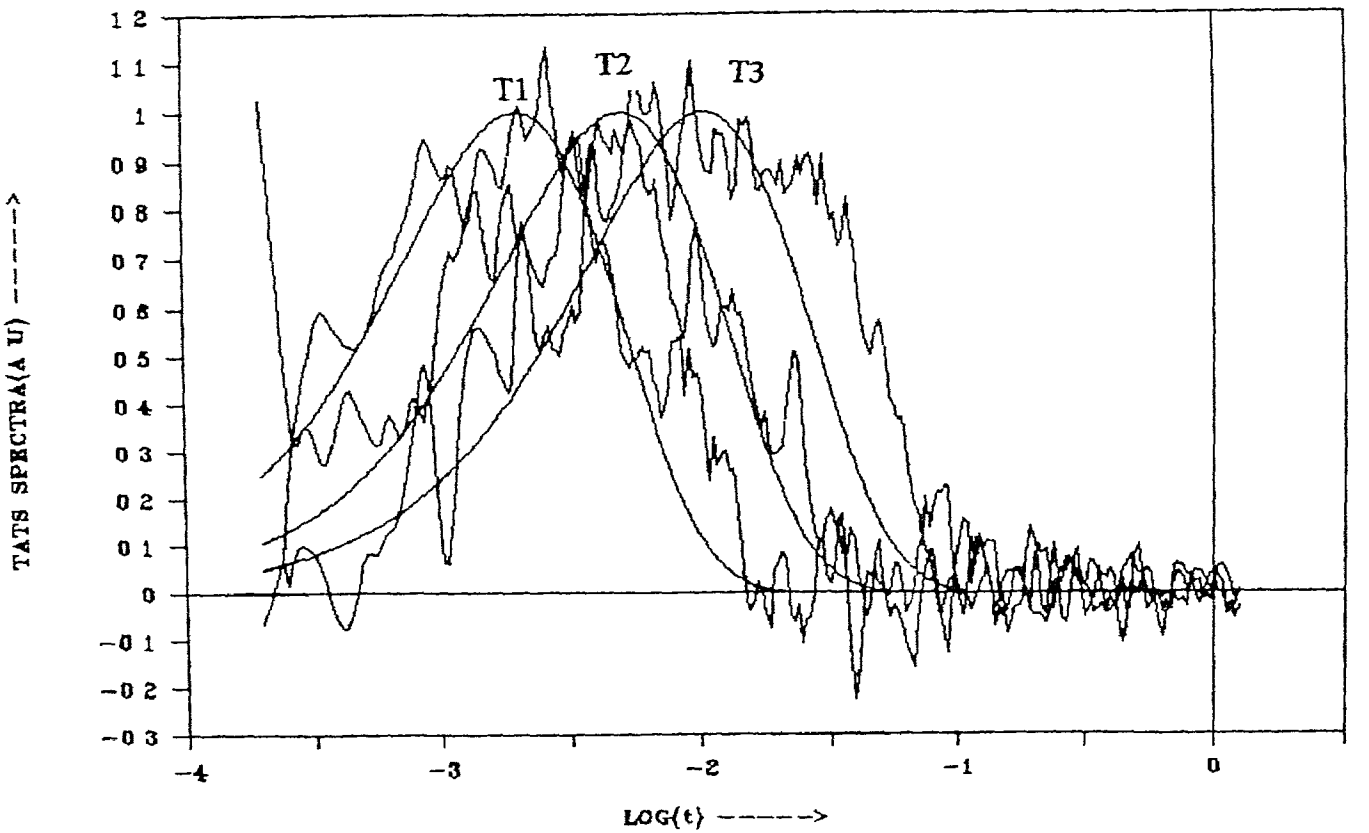

Fig 4 11 TATS spectra for ECR hyd + FA n-Si schottky diode measured at temparature (T1) 250 06 K (T2) 235 04 K (T3) 225 01 k

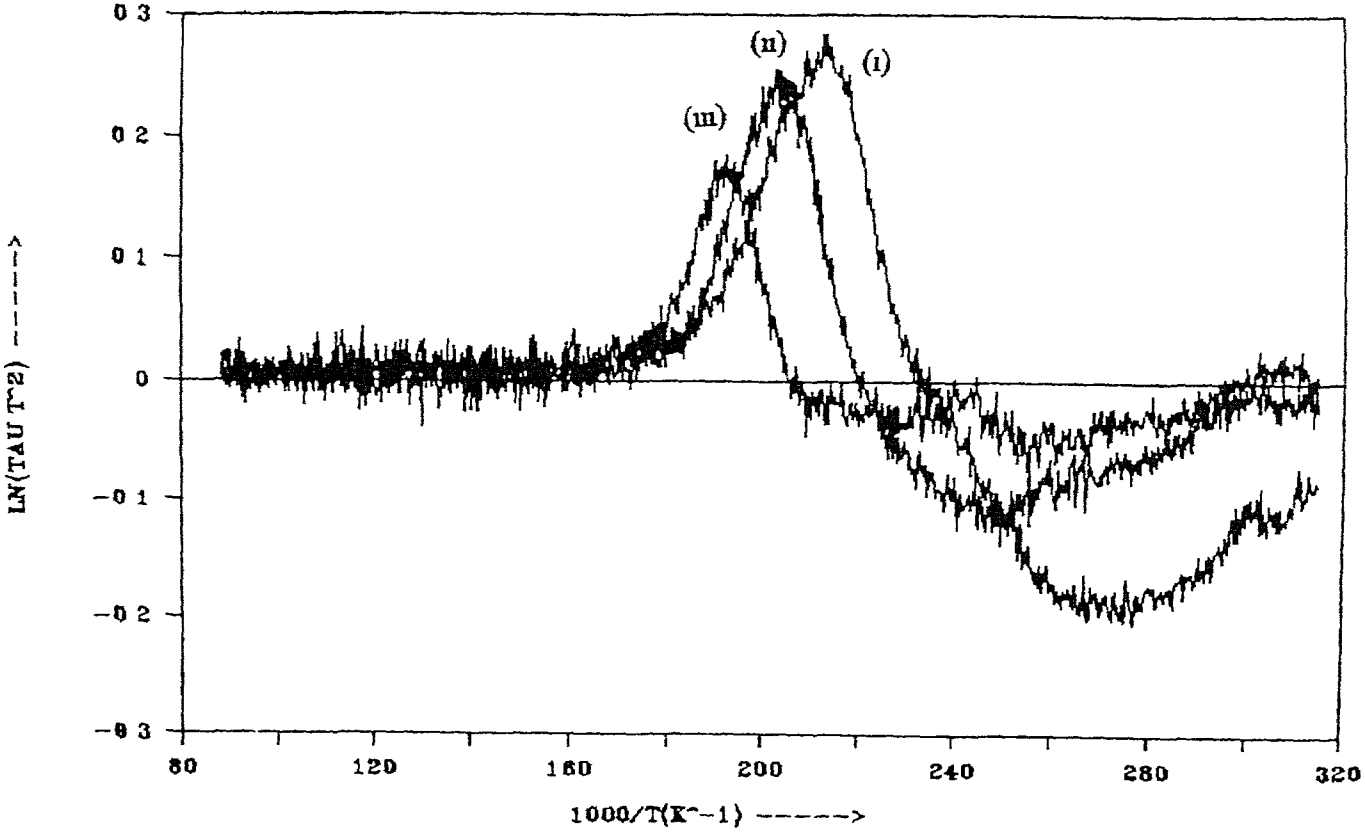

Fig 4 12 DLTS plot for Ar+ irradiated (400K) n-Si for different rate windows (i) 4 33 ms (ii) 15 87 ms & (iii) 128 ms

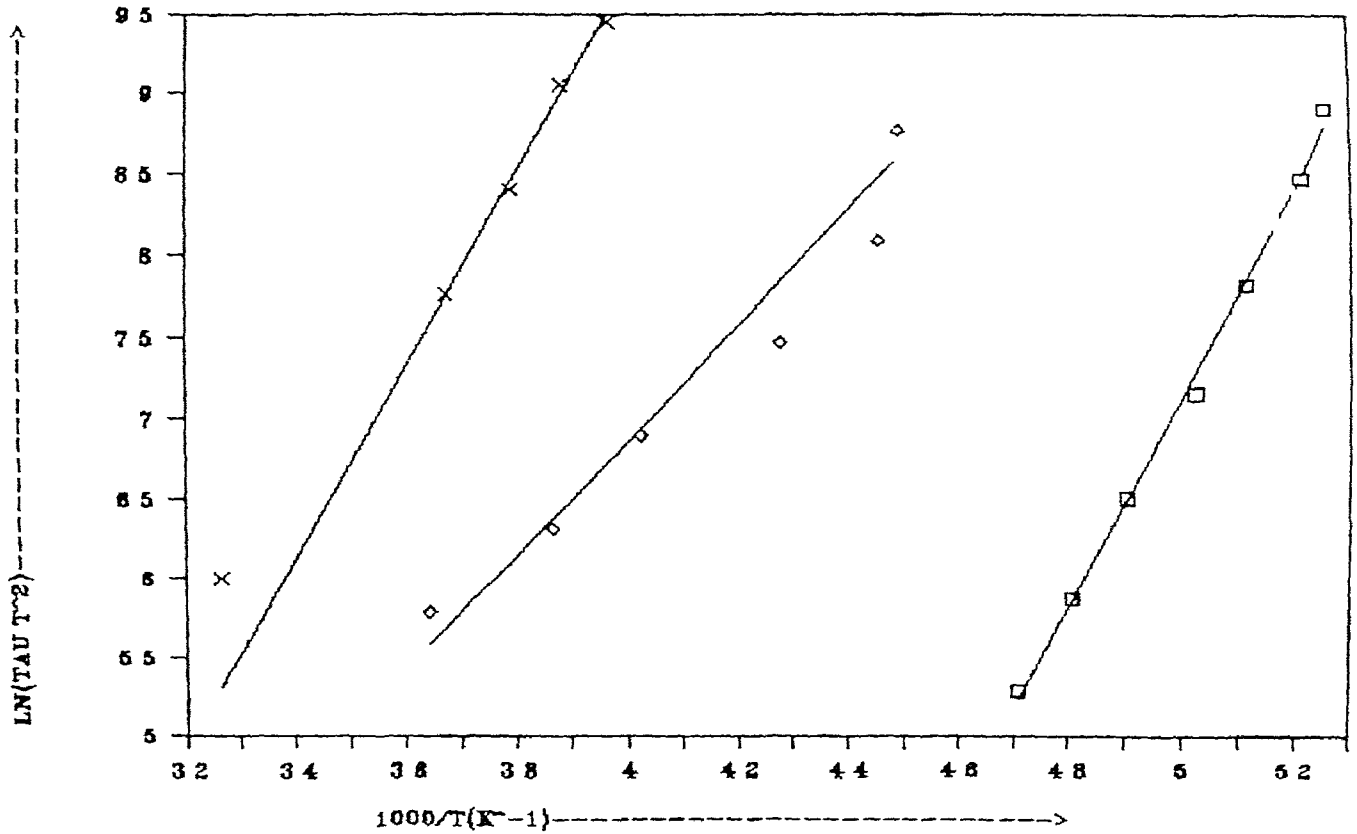

Fig 4 13 Arrhenius plot for Ar+ irradiated (400K) n-Si by DLTS signal

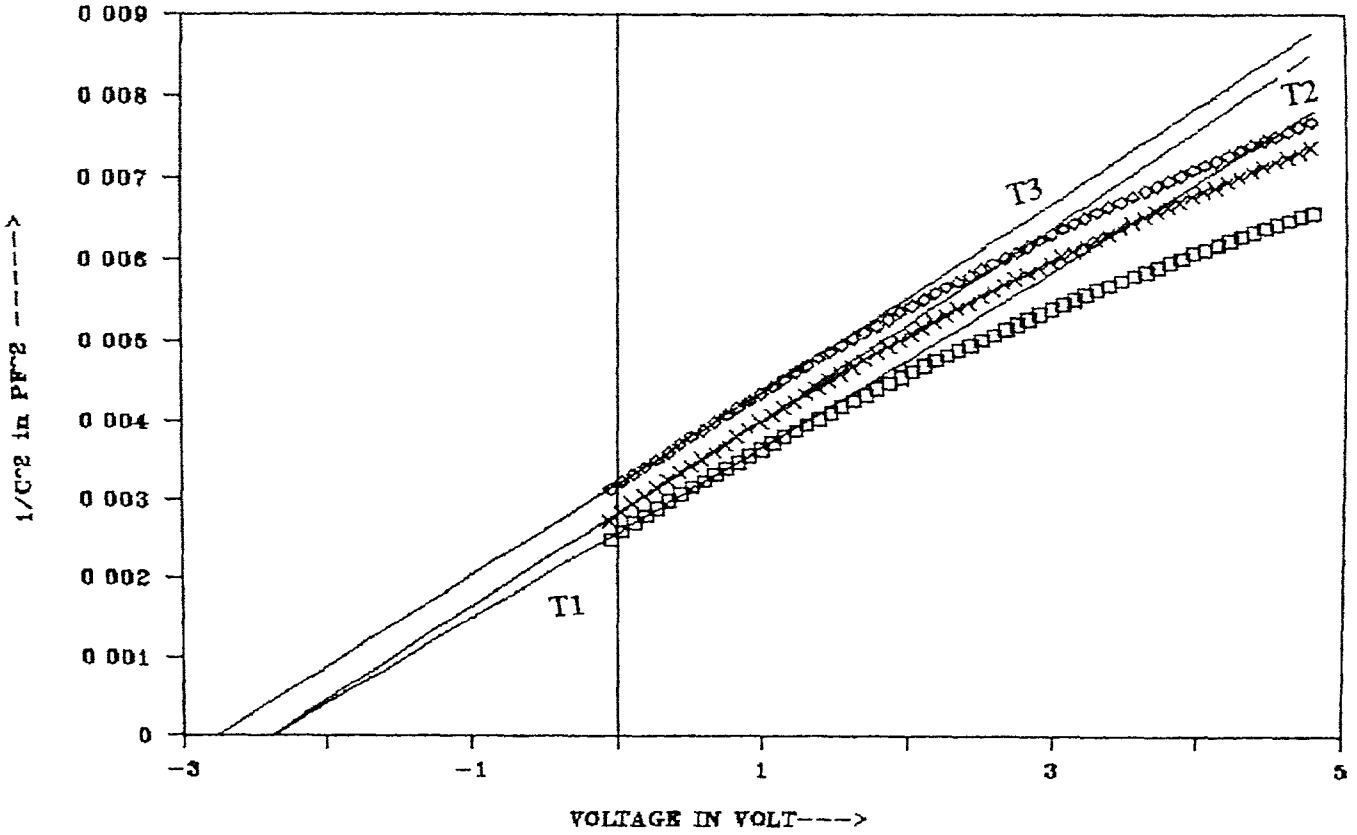

Fig 4 14 Typical C-V charecteristics of ECR hydrogenation + No anneal p-Si schottky device measured at temparature (T1) 291 9K (T2) 254 98K & (T3) 90 74 K

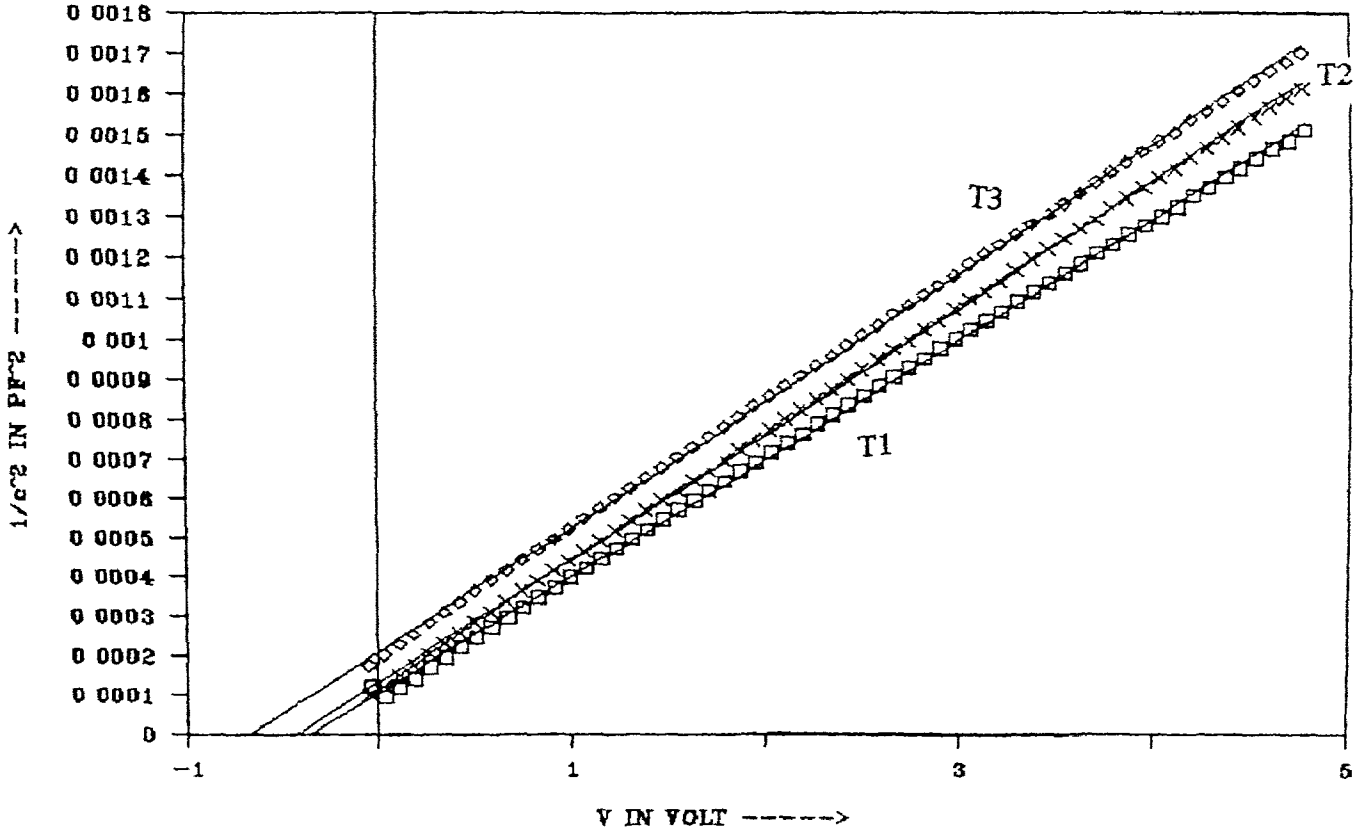

Fig 4 15 Typical C-V charecteristics of ECR hydrogenated + RTA annealing p-Si schottky device measured at temparature (T1) 291 66 K (T2) 240 63 K & (T3) 91 24 K

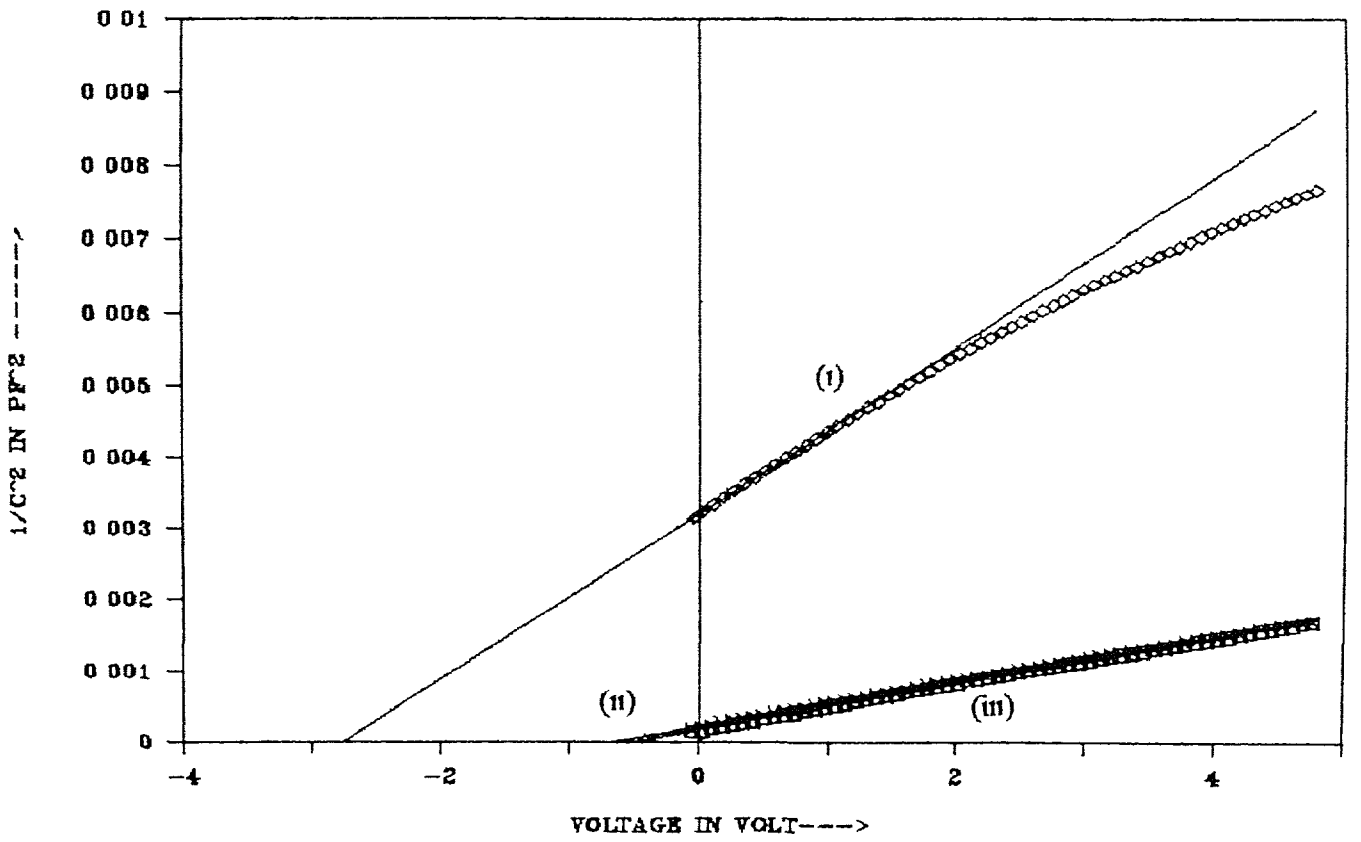

Fig 4 16 Comparision of low temp C-V charecteristics for (i) ECR hyd +No anneal (ii) ECR hyd + RTA anneal & (iii) ECR hyd + FA

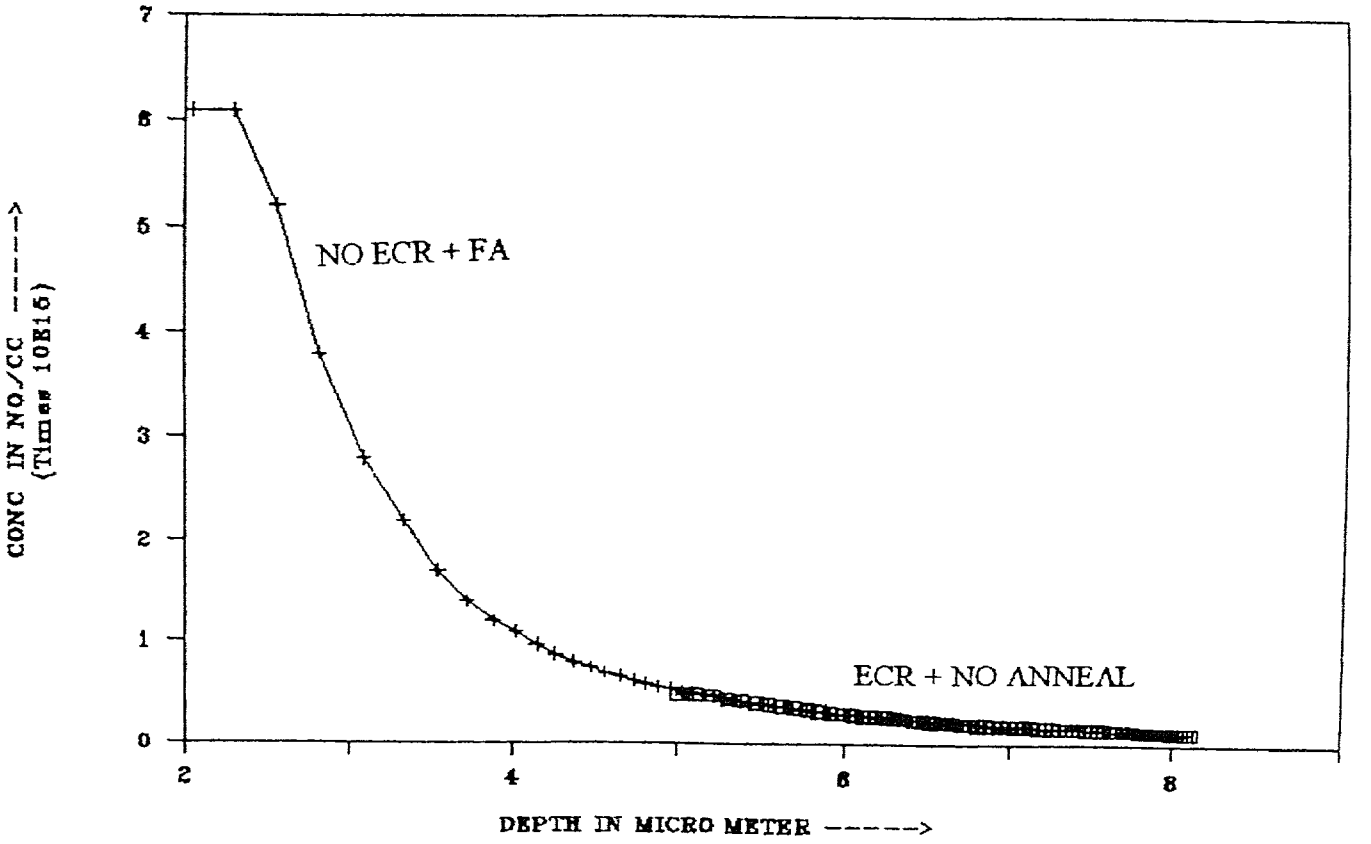

Fig 4 17 (a) Comparision of depth profile of ECR hyd + No anneal & NO hyd + FA p-Si

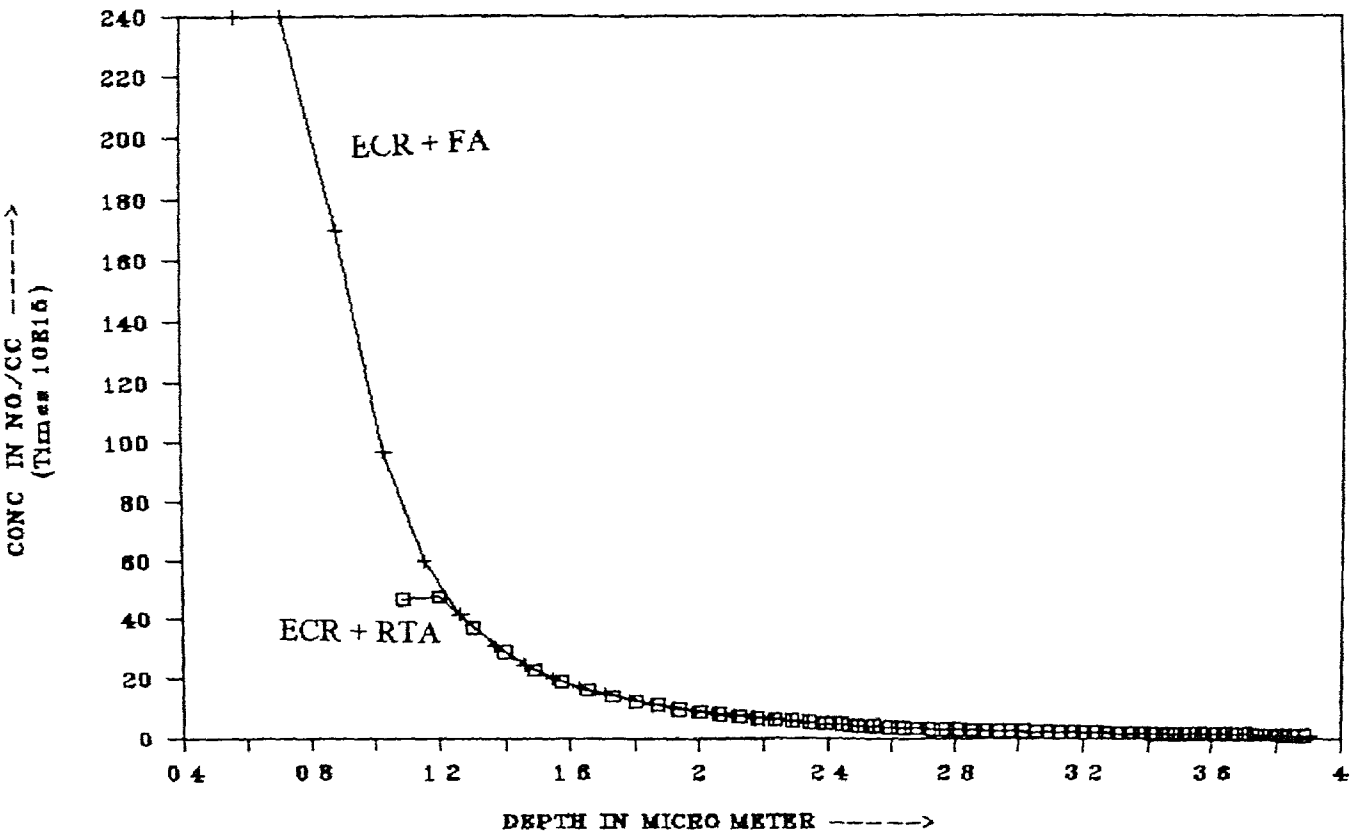

Fig 4 17 (b) Comparision of depth profile of ECR hyd + RTA anneal &

ECR hyd + FA $p\text{-}S_1$

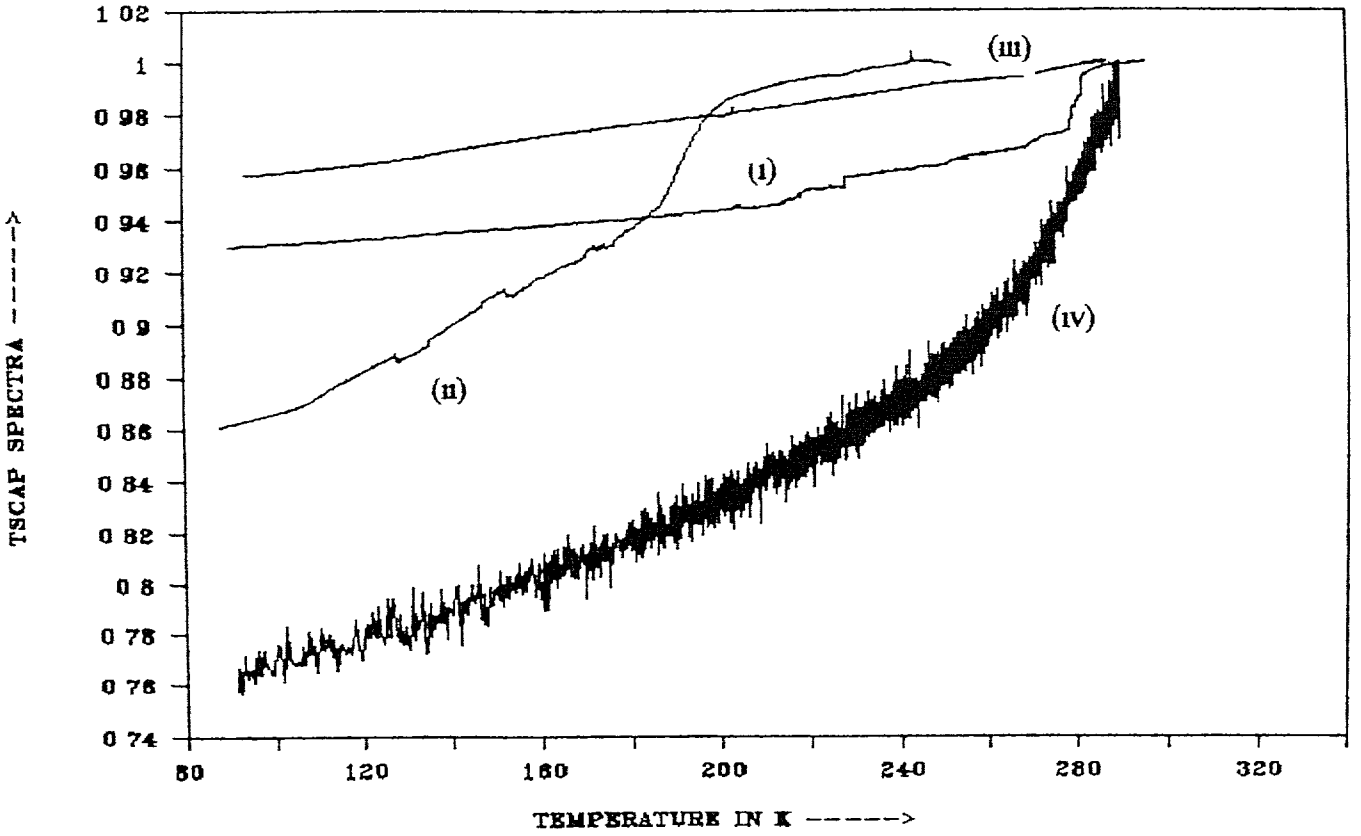

Fig 4 18 Comparision of TSCAP spectra for different p- type samples

(i) ECR + NO ANNEAL

(ii) NO ECR + FA

(iii) ECR + FA

(iv) ECR + RTA

TABLE 3 1(a)
SAMPLE CODE AND SPECIFICATION
FOR P- TYPE SAMPLES

SAMPLE CODE	TYPE	SPECIFICATION	CONDITION
PEPI FA2	P TYPE EPI Si	NO HYDROGENATION	ANNEALING BY 500^0 C FOR 30 MIN
PED CO	P TYPE EPI Si	600 W HYDROGENATION FOR 40 MIN	NO ANNEALING
PED FA1	P-TYPE EPI Si	600 W ECR HYDROGENATION FOR 40 MIN	FURNACE ANNEAL 500^0 C FOR 10 MIN
PED-R5	P TYPE EPI Si	600 W ECR HYDROGENATION FOR 40 MIN	RTA ANNEAL 500^0 C FOR 5 SEC

TABLE 3 1(b)
SAMPLE CODE AND SPECIFICATION
FOR N- TYPE SAMPLES

SAMPLE CODE	TYPE	SPECIFICATION	CONDITION
NEPI FA1	N TYPE EPI Si	NO HYDROGENATION	ANNEAL 500^0 C FPR 5 SEC
NED CO	N-TYPE EPI Si	600W ECR HYDROGENATION FOR 60 MIN	NO ANNEAL FOLLOWED
NED FA1	N TYPE EPI Si	600 W ECR HYDROGENATION FOR 40 MIN	FURNACE ANNEAL 500^0 C FOR 10 MIN
NED -R5	N TYPE EPI Si	600 W ECR HYDROGMIN	RTA ANNEAL BY 500^0 C FOR 5 SEC

TABLE -4 2

TABULATION FOR THE RANGE OF DEPTH THAT CAN BE SCANNED IN N-TYPE Si SAMPLES (AT ROOM TEMPERATURE & AT LOW TEMPERATURE)

SAMPLE (N Si) SPECIFICATION	RANGE (μm) ROOM TEMPERATURE	RANGE (μm) LOW TEMPERATURE
1 NED CO (ECR + NO ANNEAL)	2 22 3 15	1 6 3 2
2 NED FA1 (ECR + FA)	9 21 12 61	16 7 18 1
3 NED R5 (ECR + RFA)	0 8 2 36	1 0 2 6
4 NEPI I A1 (NO ECR + FA)	0 75 2 33	0 8 2 4

TABLE 4 2

COMPARISION OF ENERGY & CAPTURE CROSS SECTION OF THE MINORITY DEFECT N TYPE Si (FA + ECR)

EXPERIMENT	ENERGY(ev)	CAPTURE CROSS SECTION(CM^2)
DLTS	0 386	$3\ 2 \times 10^{16}$
TATS	0 32	$2\ 6 \times 10^{17}$

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